

6 V to 28 V, 1.2 A 1ch

Step-Down Switching Regulator Integrated Power MOSFET

BD9E151ANUX

General Description

BD9E151ANUX is diode-rectification buck converter of high input voltage 28 V with integrated Power MOSFET. Because of diode-rectification, a pulse skips in light load automatically and it maintains high efficiency. In addition, it is available for battery powered application because supply current is small with 0 uA at shutdown. It can easily make a small power supply with the external parts of the wide range, because the use of ceramic capacitor is possible, and because it has high speed road response by current mode control and has the external setting phase compensation.

Key Specifications

- Input Voltage Range: 6 V to 28 V
- Reference Voltage Precision (Ta = 25 °C): 1 V ± 1.0 %
- Max Output Current: 1.2 A (Max)
- Operating Temperature Range: -40 °C to +85 °C

Package

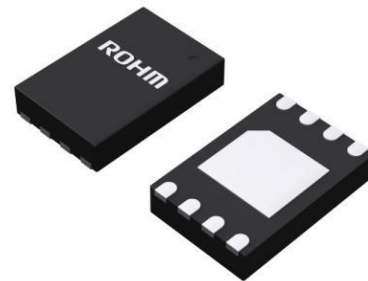
VSON008X2030

W (Typ) x D (Typ) x H (Max)

2.0 mm x 3.0 mm x 0.6 mm

Features

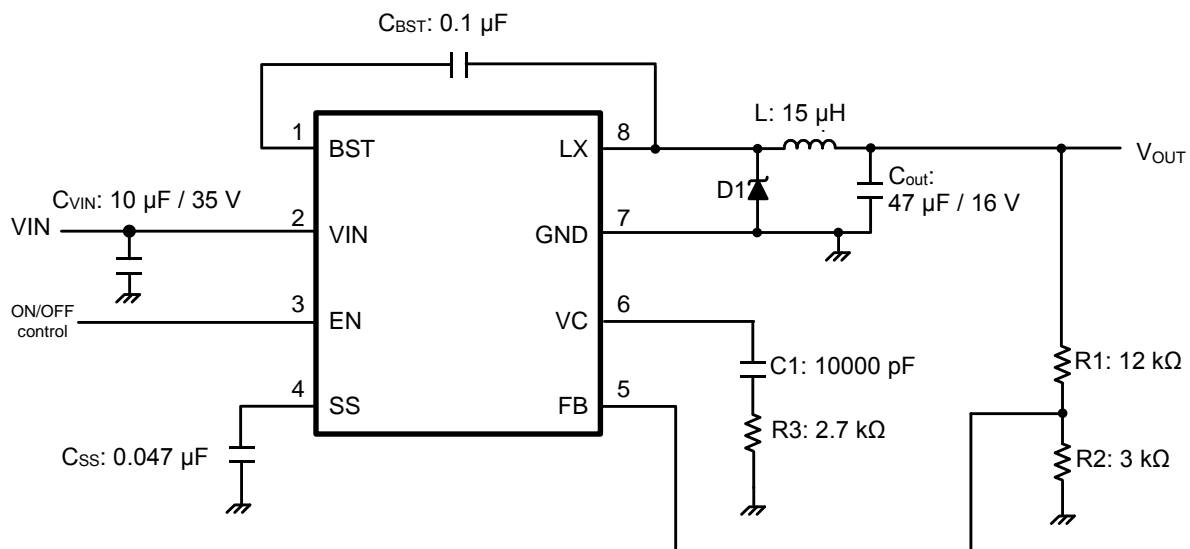
- Wide Input Range (VIN = 6 V to 28 V)
- 30 V / 80 mΩ Integrated Power MOSFET
- 600 kHz (Typ) High Frequency Operation
- Built in Reference Voltage (1.0 V ± 1.0 %)
- Built in Over Current Protection (OCP), Under Voltage Lockout (UVLO), Over Voltage Protection (OVP), Thermal Shutdown (TSD)
- Stand-by mode (IIN = 0 μA)
- VSON008X2030 Small Package



Applications

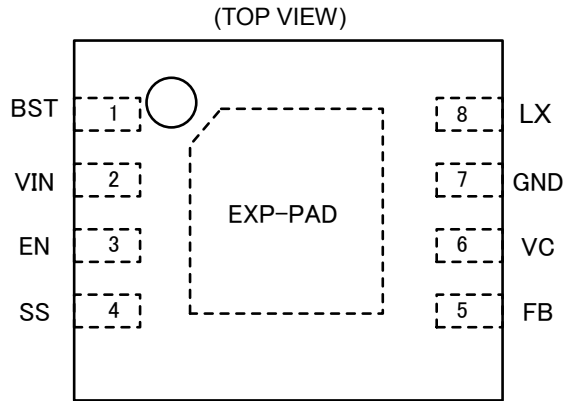
- Surveillance Camera Applications
- Consumer 12 V, 24 V BUS-Line Systems
- OA Applications

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

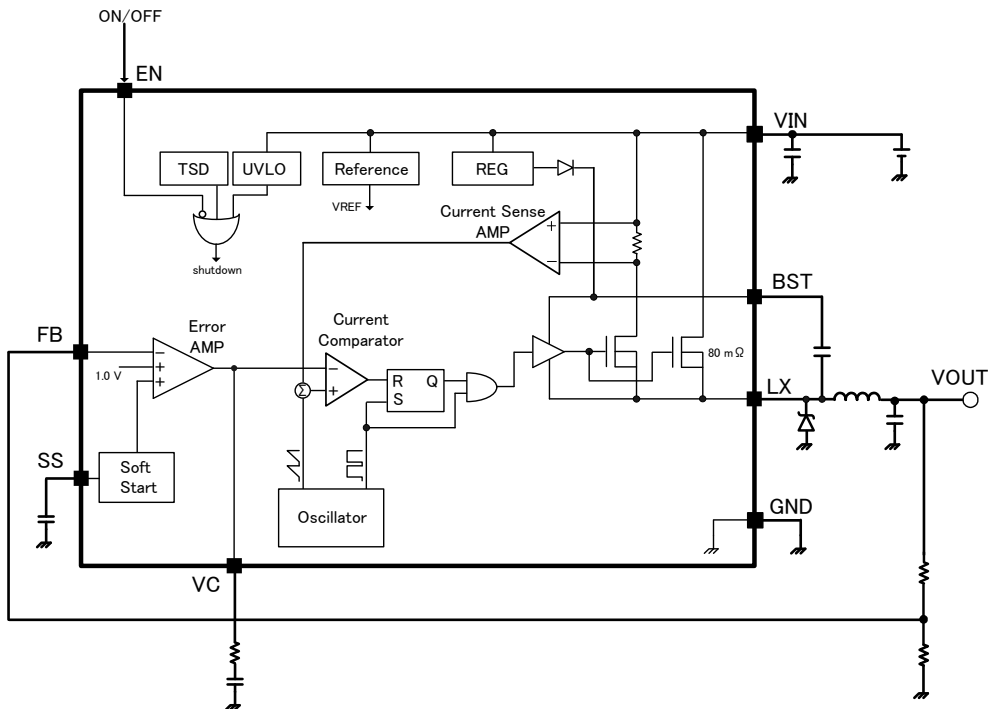
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	BST	Bootstrap Capacitor Connecting Pin
2	VIN	Input Supply Pin
3	EN	EN Pin
4	SS	Soft Start Setting Pin
5	FB	Feedback Input Pin
6	VC	Error AMP Output Pin
7	GND	Ground
8	LX	Switching Pin
-	EXP-PAD	The EXP-PAD connect to GND

Block Diagram



Description of Blocks

1. Reference
This block generates reference voltage. It starts operation by EN pin High.
It provides reference voltage to error amplifier reference voltage 1.0 V (Typ), reference of oscillator, and etc.
2. REG
This is a gate drive and regulator for internal circuit power supply.
3. Oscillator
This is an oscillation circuit with operation frequency fixed to 600 kHz (Typ).
4. Soft Start
This is a circuit that gently raises the output voltage of the DC / DC converter to prevent in-rush current during start-up.
Soft start time is determined by the capacitor connected to SS pin and SS pin charge current.
5. Error AMP
This is an error amplifier circuit that detects the output signal, and outputs PWM control signal.
Internal reference voltage is set to 1.0 V (Typ).
6. OVP
Output voltage is monitored with the FB pin, and output FET is turned off when it becomes 110 % or more of setting value.
When the output voltage becomes 105 % or less, it makes possible to turn on FET again.
7. Current Comparator
This is comparator that outputs PWM signal from current feed-back and error amp output for current mode.
8. OCP
Current flowing FET is monitored, and output FET is turned off when it detects over current 2.2 A (Typ).
When over current is detected for two consecutive cycles, the device is turned off with latch.
Then the SS pin voltage and VC pin voltage is reset, and the device is automatically restarted when the SS pin voltage reaches 0.1 V.
9. Power MOSFET
This is power MOSFET with maximum voltage 30 V and on-resistance 80 mΩ.
It should be used within 1.6 A including ripple current of inductor because the current limiting of power MOSFET is 1.6 A.
10. UVLO
This is a low voltage error prevention circuit.
This prevents internal circuit error during increase and decrease of power supply voltage.
VIN pin voltage is monitored, and it turns off output FET and resets Soft Start circuit when VIN voltage becomes UVLO detect threshold or less. UVLO detect threshold has hysteresis.
11. TSD
This is over thermal protection circuit.
When it detects the temperature exceeding maximum junction temperature ($T_{jmax} = 150\text{ }^{\circ}\text{C}$), it turns off the output FET, and resets Soft Start circuit. When the temperature decreased, It has hysteresis and the device is automatically restarted.
12. EN
When Voltage 2.4 V or more is supplied to this pin, it turns on. When open or voltage 0.8V or less is supplied, it turns off.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{IN}	30	V
BST – GND	V _{BST}	37	V
BST – LX	ΔV _{BST}	7	V
EN – GND	V _{EN}	30	V
LX – GND	V _{LX}	30	V
FB – GND	V _{FB}	7	V
VC – GND	V _{VC}	7	V
SS – GND	V _{SS}	7	V
Power MOSFET Current	I _{DH}	1.6	A
Maximum Junction Temperature	T _{jmax}	150	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
VSON008X2030				
Junction to Ambient	θ _{JA}	308.3	69.6	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ _{JT}	43	10	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 5) This thermal via connects with the copper pattern of all layers. The arrangement should follow to land patterns.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{IN}	6	-	28	V
Output Voltage	V _{OUT}	1.0 (Note 6)	-	V _{IN} × 0.7 or V _{IN} - 5 (Note 7)	V
Output Current	I _{OUT}	-	-	1.2	A
Operating Temperature	T _{opr}	-40	+25	+85	°C

(Note 6) Restricted by minimum on pulse typ. 100 nsec.

(Note 7) Restricted by BSTUVLO or Max Duty Cycle (ref. p.14). Please set value of the low one for the maximum.

Electrical Characteristics (Unless otherwise specified V_{IN} = 12 V, V_{OUT} = 5 V, EN = 5 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	
Circuit Current							
Stand-by Current of V _{IN}	I _{ST}	-	0	10	μA	V _{EN} = 0 V	
Operating Circuit Current of V _{IN}	I _{IN}	-	0.8	1.6	mA	V _{FB} = 1.5 V	
Undervoltage Lockedout							
Reset Threshold Voltage	V _{UV}	5.0	5.4	5.8	V	V _{IN} rising	
Hysteresis Width	V _{UVHY}	-	200	400	mV		
Oscillator							
Oscillating Frequency	f _{SW}	540	600	660	kHz		
Max Duty Cycle	D _{MAX}	85	91	-	%		
Error AMP							
FB Threshold Voltage	V _{FBTH}	0.990	1.000	1.010	V		
FB Input Current	I _{FB}	-1.0	0	1.0	μA	V _{FB} = 0 V	
DC Gain	A _{VEA}	-	600	6000	V/V		
Transconductance	G _{EA}	-	250	500	μA/V	I _{VC} = ±10 μA, V _{VC} = 1.0 V	
Current Sense Amplifier							
Transconductance	G _{CS}	-	10	20	A/V		
Output							
High-Side Power MOSFET ON Resistance	R _{ONH}	-	80	160	mΩ		
High-Side Over Current Detect Current	I _{OCP}	1.6	2.2	-	A		
CTL							
EN Threshold Voltage	ON	V _{ENON}	2.4	-	V _{IN}	V	Ta = -40 °C to +85 °C V _{IN} = 6 V to 28 V
	OFF	V _{ENOFF}	-0.3	-	0.8	V	
EN Input Current	I _{EN}	6.0	7.0	15.0	μA	V _{EN} = 5 V	
SOFT START							
Charge Current	I _{SS}	1	2	4	μA		

Typical Performance Curves

(Unless otherwise specified $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $EN = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

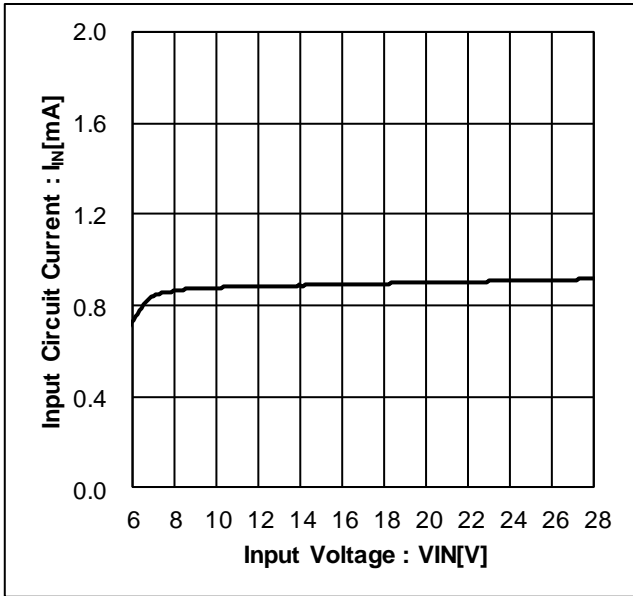


Figure 1. Input Circuit Current vs Input Voltage

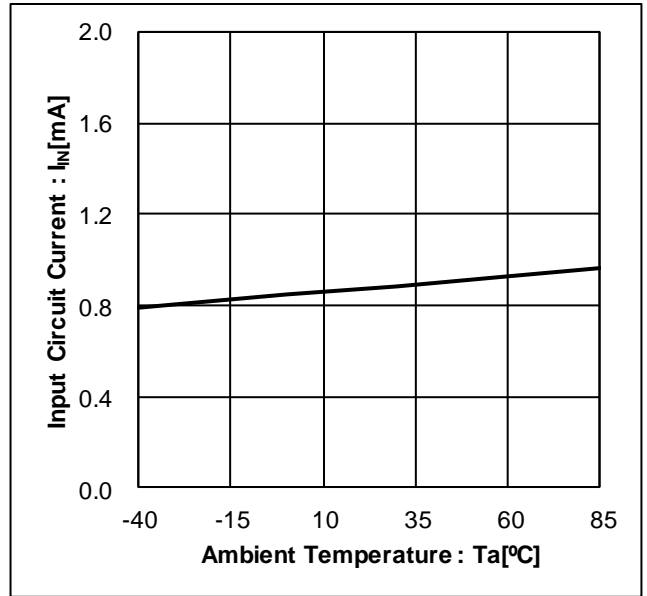


Figure 2. Input Circuit Current vs Ambient Temperature

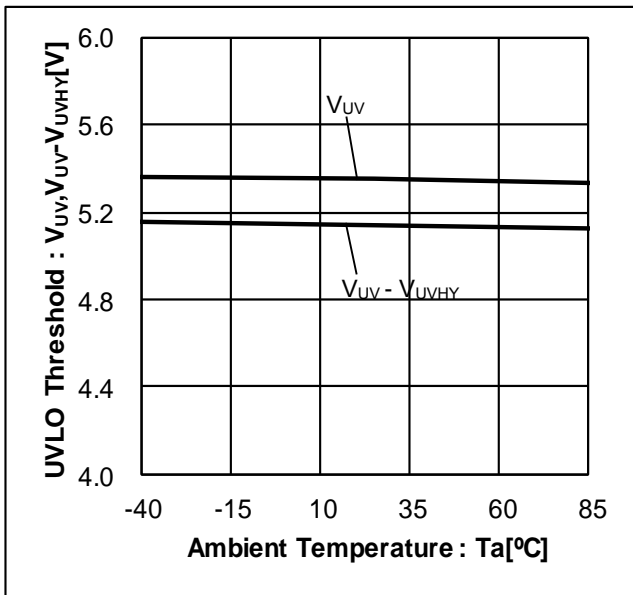


Figure 3. UVLO Threshold vs Ambient Temperature

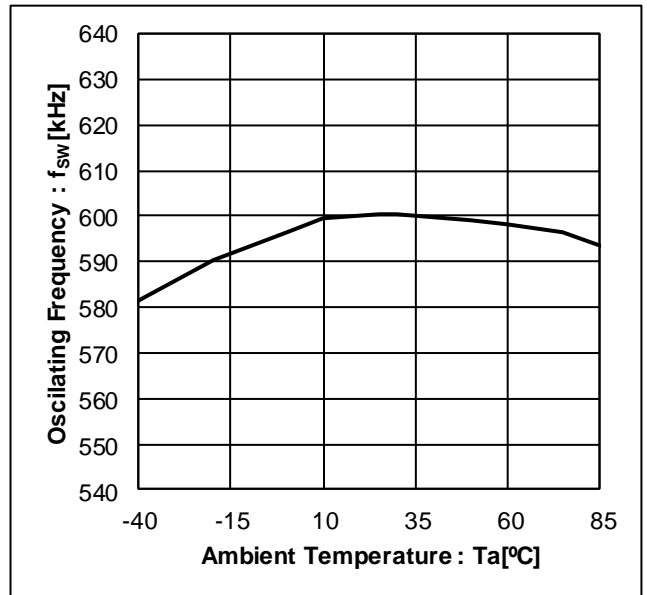


Figure 4. Oscillating Frequency vs Ambient Temperature

Typical Performance Curves – Continued

(Unless otherwise specified $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $EN = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

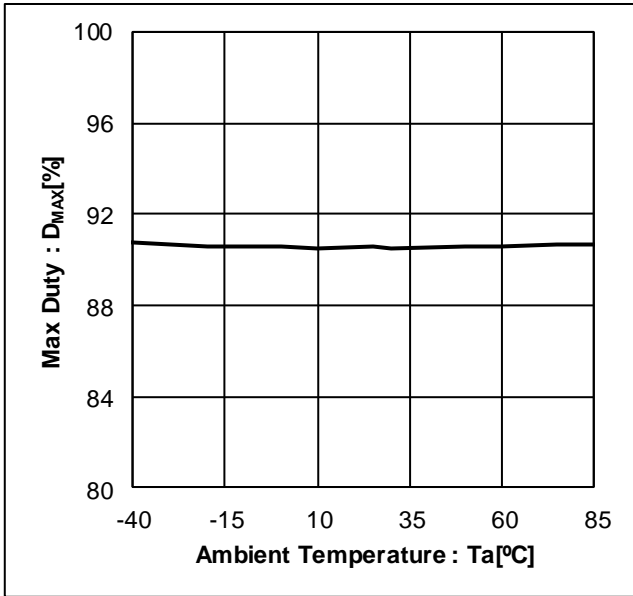


Figure 5. Max Duty vs Ambient Temperature

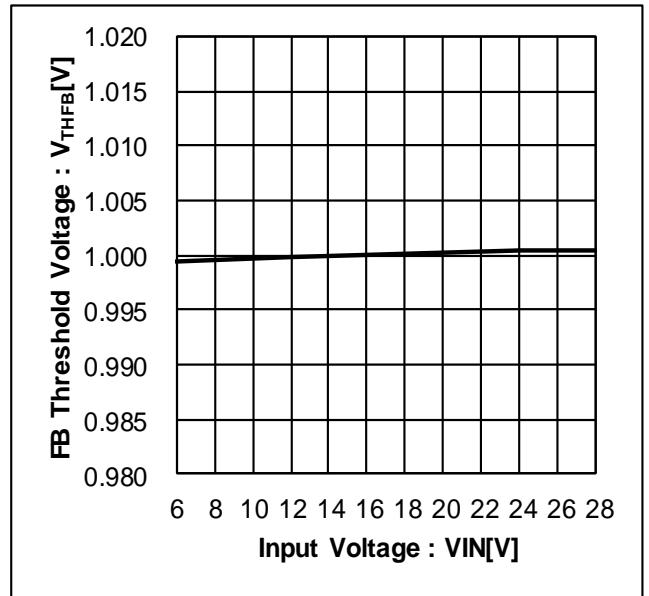


Figure 6. FB Threshold Voltage vs Input Voltage

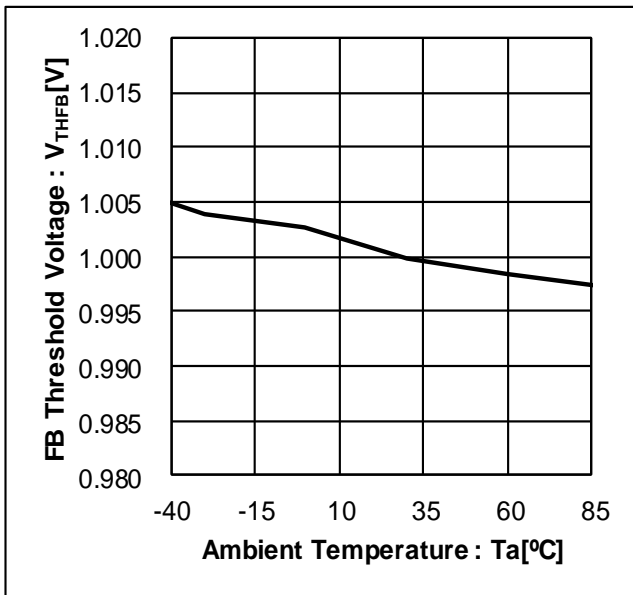


Figure 7. FB Threshold Voltage vs Ambient Temperature

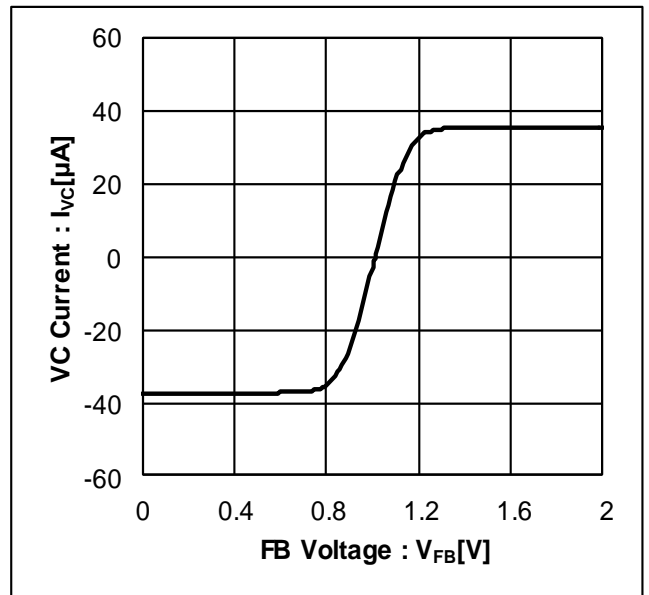


Figure 8. VC current vs FB Voltage

Typical Performance Curves – Continued

(Unless otherwise specified $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $EN = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

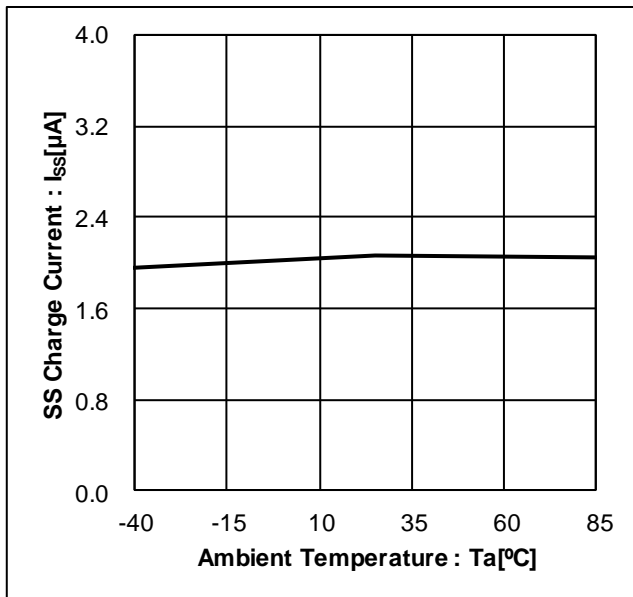


Figure 9. SS Charge Current vs Ambient Temperature

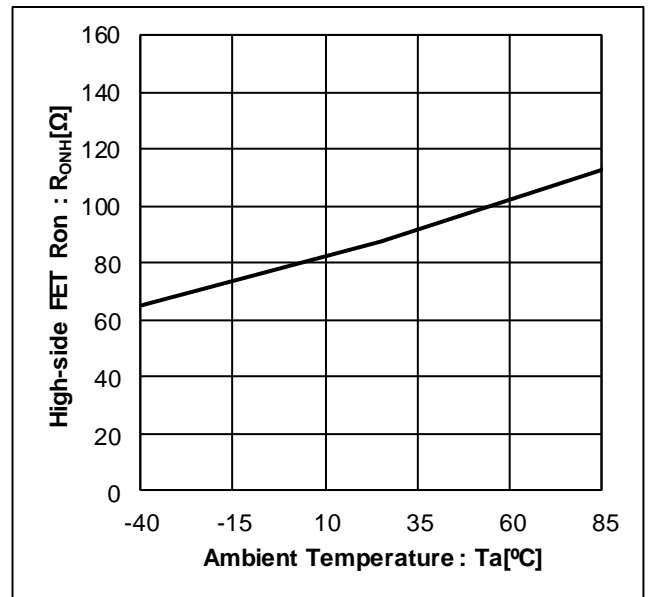


Figure 10. High-Side FET Ron vs Ambient Temperature

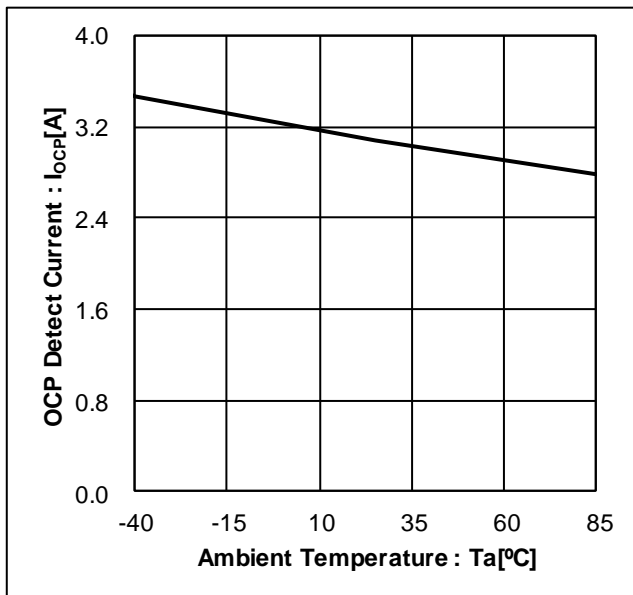


Figure 11. OCP Detect Current vs Ambient Temperature

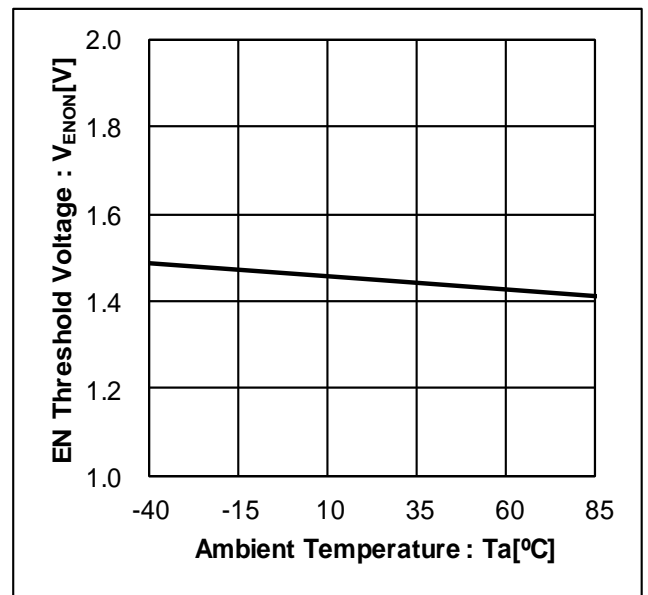


Figure 12. EN Threshold Voltage vs Ambient Temperature

Typical Application

VIN = 12 V, VOUT = 5 V, IOUT = 1 A

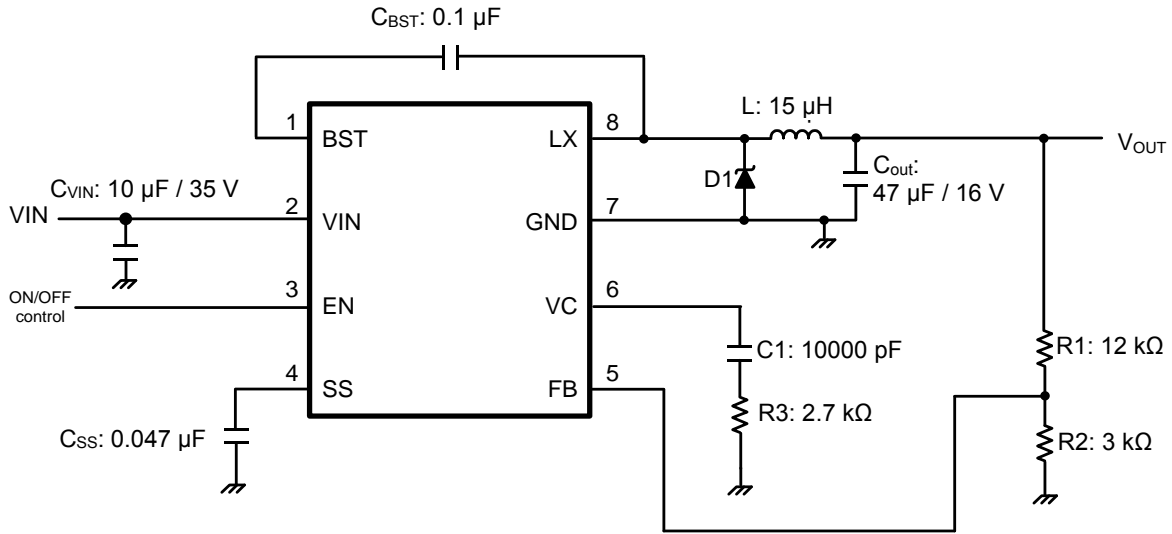


Figure 13. Typical Application Schematic (VOUT = 5 V)

When use in VIN < 7 V is assumed, it is recommended to add to pull-down resistance of about 1 kΩ to VOUT as shown above.

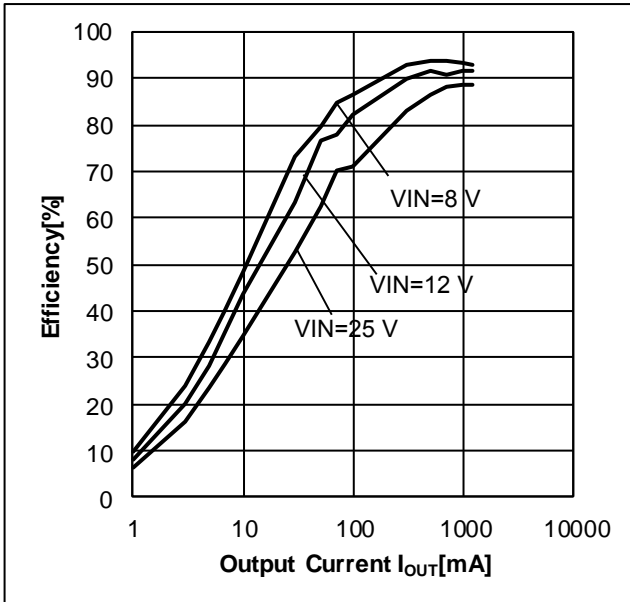


Figure 14. Efficiency vs Output Current

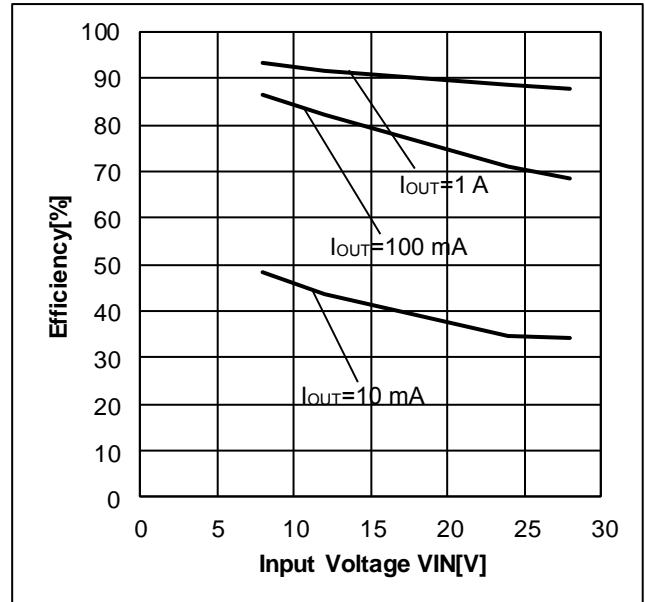


Figure 15. Efficiency vs Input Voltage

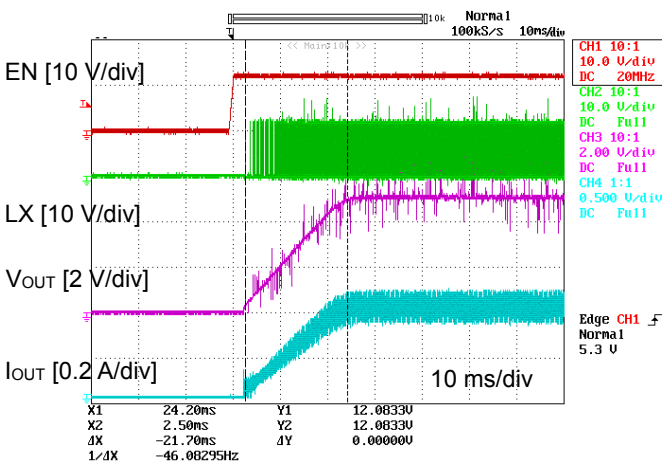


Figure 16. Start-up Waveform

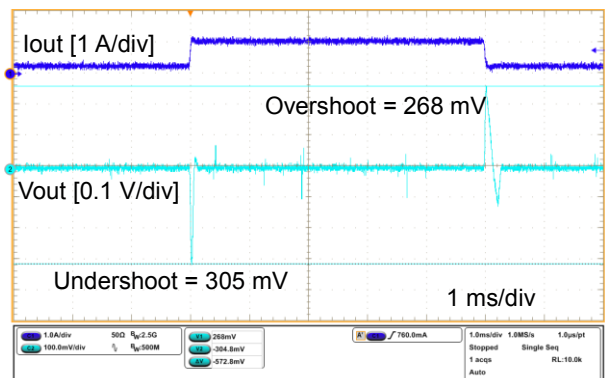


Figure 17. Load Transient Characteristic

Typical Application – Continued

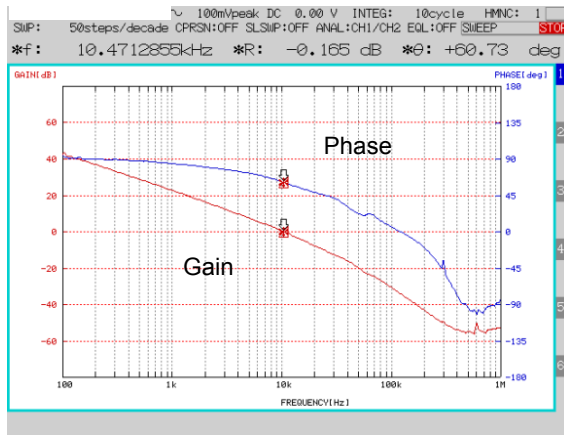


Figure 18. Frequency Characteristic ($I_{OUT} = 1\text{ A}$)

Typical Application – Continued

Application Parts List 1 ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$)

Symbol	Value	Parts name	Company
[Capacitor]			
C_{VIN}	10 μF / 35 V	GRM21BR6YA106KE43	MURATA
C_{SS}	0.047 μF / 25 V	GRM155R71E473JA88	MURATA
C1	10000 pF / 25 V	GRM033B31E103KA12	MURATA
C_{BST}	0.1 μF / 10 V	GRM033B31A104ME84	MURATA
C_{OUT}	47 μF / 16 V	GRM32EC81C476KE15	MURATA
[Resistor]			
R3	2.7 k Ω	MCR03 series	ROHM
R4	12 k Ω	MCR03 series	ROHM
R5	3 k Ω	MCR03 series	ROHM
[Diode]			
D	-	RSX201VAM-30	ROHM
[Inductor]			
L	15 μH	NRS6045T150	TAIYO YUDEN

Application Parts List 2 (When load current is light and total area is important) ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 300\text{ mA}$)

Symbol	Value	Parts name	Company
[Capacitor]			
C_{VIN}	10 μF / 25 V	GRM188R61E106MA73	MURATA
C_{SS}	0.047 μF / 25 V	GRM155R71E473JA88	MURATA
C1	22000 pF / 25 V	GRM155R71H223JA61	MURATA
C_{BST}	0.1 μF / 10 V	GRM033B31A104ME84	MURATA
C_{OUT}	22 μF / 10 V	GRM31CR71A226ME15	MURATA
[Resistor]			
R3	2.2 k Ω	MCR006 series	ROHM
R4	12 k Ω	MCR006 series	ROHM
R5	3 k Ω	MCR006 series	ROHM
[Diode]			
D	-	RSX201VAM-30	ROHM
[Inductor]			
L	15 μH	DEM3518C series	MURATA

Selection of External Application Components

(1) Inductor

Shield type that meets the current rating (current value from the I_{PEAK} below), with low DCR (direct current resistance element) is recommended. The value of inductor has an effect in the inductor ripple current which causes the output ripple. In the same formula below, this ripple current can be made small with a large value L of inductor or as high as the switching frequency.

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (1)$$

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (2)$$

(ΔI_L : Output ripple current, V_{IN} : Input voltage, f_{SW} : Switching frequency)

For design value of inductor ripple, please carry out design tentatively with about 20 % to 50 % of maximum output current.

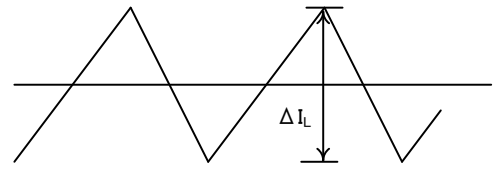


Figure 19. Inductor Current

(2) Output Capacitor

It is recommended a ceramic capacitor of low ESR for reducing output ripple.

Also, for capacitor rating, please use a capacitor that maximum rating has sufficient margin to the output voltage with taking into consideration the DC bias characteristics.

Output ripple voltage is determined by following formula.

$$V_{PP} = \Delta I_L \times \frac{1}{2\pi \times f_{SW} \times C_{OUT}} + \Delta I_L \times R_{ESR} \quad (3)$$

Please set the value within allowable ripple voltage. It is recommended a ceramic capacitor 10 μ F or more.

(3) Output Voltage Setting

Error AMP internal reference voltage is 1.0 V.

Output voltage is determined by following formula.

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{REF} \quad (4)$$

(4) Bootstrap Capacitor

Please connect ceramic capacitor from 0.047 μ F to 0.47 μ F between BST pin and LX pin.

Because the rating between BST pin and LX pin becomes 7 V, it is recommended the proof pressure 10 V or more.

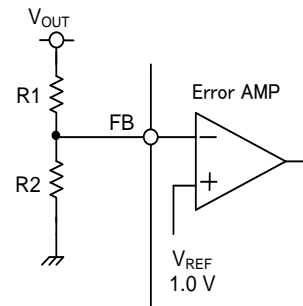


Figure 20. Output Voltage Setting

(5) Soft Start Function

BD9E151ANUX is not built in setting of soft start time.

It is necessary to set it by external capacitor C_{SS} between SS pin and GND to prevent rush current in the start-up.

BD9E151ANUX has the internal current source of 2 μ A as charging current.

Soft start time (10 % to 90 %) is determined by following formula.

The I_{SS} current is 2 μ A.

$$T_{SS} = \frac{C_{SS} \times 0.8}{I_{SS}} \quad (5)$$

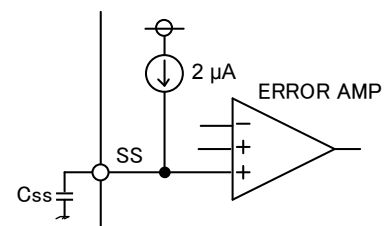


Figure 21. Soft Start Time Setting

(6) Catch Diode

BD9E151ANUX needs to connect an external catch diode between LX and GND. It is necessary for the diode to choose to satisfy absolute maximum ratings of the application. The reverse voltage must be higher than the maximum voltage ($V_{INMAX} + 0.5$ V) of the LX pin. The peak current needs to be larger than $I_{OUTMAX} + \Delta I_L$.

Selection of External Application Components – Continued

(7) Input Capacitor

BD9E151ANUX needs an input decoupling capacitor. It is recommended a low ESR ceramic capacitor of 10 uF or more. The capacitor is selected considering DC bias effect and temperature characteristic. Please place this capacitor as possible as close to the VIN pin.

The input ripple voltage is estimated by following formula.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{VIN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{6}$$

C_{VIN} is input capacitor value

It is necessary to confirm RMS ripple current. The RMS current is estimated by following formula.

$$I_{CVIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{7}$$

IC_{VIN} has maximum value when VIN = 2 × V_{OUT}. The value is estimated by following formula.

$$I_{CVINMAX} = \frac{I_{OUT}}{2} \tag{8}$$

(8) About Adjustment of DC/DC Converter Frequency Characteristic

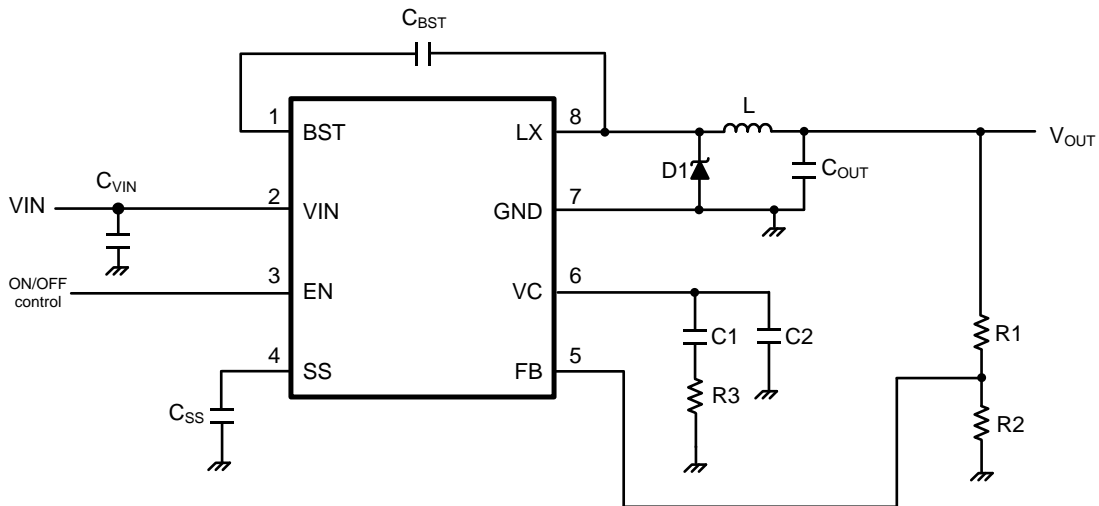


Figure 22. Role of Phase Compensation element

Stability and responsiveness of loop are controlled through the VC pin which is the output of Error AMP. The characteristic of zero and pole that determines stability and responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC pin. (C1, C2, R3)

DC gain of voltage return loop can be calculated by following formula.

$$A_{dc} = R_l \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}} \tag{9}$$

V_{FB} is feedback voltage (Typ: 1.0 V).
 A_{EA} is voltage gain of Error AMP (Typ: 60 dB).
 G_{CS} is transconductance of current detect (Typ: 10 A/V).
 R_l is output load resistance value.

Selection of External Application Components – Continued

There are 2 poles in the control loop of BD9E151ANUX.

The first occurs with through the output resistance of phase compensation capacitor (C1).

The other one occurs with through the output capacitor and load resistance.

These poles appear at the following frequency.

$$f_{P1} = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}} \quad (10)$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_L} \quad (11)$$

where:

G_{EA} is the transconductance of Error AMP (Typ: 250 $\mu A/V$).

This control loop has a zero.

The zero which occurs by phase compensation capacitor C1 and phase compensation resistance R3 appears at the following frequency.

$$f_{Z1} = \frac{1}{2\pi \times C1 \times R3} \quad (12)$$

Also, if output capacitor is large, and that ESR (R_{ESR}) is large, it has additional zero (ESR zero).

This ESR zero occurs by ESR of output capacitor and capacitance, and exists at the following frequency.

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (\text{ESR Zero}) \quad (13)$$

In this case, the 3rd pole that determined with the 2nd phase compensation capacitor (C2 is the capacitor between VC and GND) and phase correction resistance (R3) is used to correct the effect of ESR zero in the loop gain.

This pole exists at the following frequency.

$$f_{P3} = \frac{1}{2\pi \times C2 \times R3} \quad (\text{Pole that corrects ESR Zero}) \quad (14)$$

The target of phase compensation design is to have the necessary band width and phase margin.

Cross-over frequency (band width: f_C) is set so that loop gain of return loop becomes zero.

When cross-over frequency becomes low, power supply fluctuation response and load response become worse.

When cross-over frequency becomes high, phase margin of the loop decreases.

To have the phase margin, cross-over frequency needs to set 1/20 of switching frequency or less.

Setting method of phase compensation value is shown below.

1. Phase compensation resistor (R3) matching the desired cross-over frequency is selected. R3 is calculated using the following formula.

$$R3 = \frac{2\pi \times C_{OUT} \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (15)$$

2. Phase compensation capacitor (C1) is selected. It has enough phase margin by matching zero of compensation to 1/4 or less of the cross-over frequency. C1 is calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times f_C} \quad (16)$$

Selection of External Application Components – Continued

3. This is considered if the 2nd phase compensation capacitor C2 is need. If the ESR zero of output capacitor smaller than half of the switching frequency, the 2nd phase compensation capacitor is necessary. In other words, it is the case that the following formula holds.

$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_{SW}}{2} \quad (17)$$

In this case, add the second phase compensation capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

$$C2 = \frac{C_{OUT} \times R_{ESR}}{R3} \quad (18)$$

Output Voltage Restriction

BD9E151ANUX have a function of BSTUVLO to prevent malfunction at low voltage between BST and LX. Therefore OUTPUT voltage is restricted by BSTUVLO and Max Duty Cycle (Min 85 %).

1. Restriction by BSTUVLO

When the voltage between BST and LX is lower than 2.5 V, High-Side FET will be made turned off and the charge will provide from VIN to BST directly to reset BSTUVLO (Path 1). The below formula is needed to be satisfied to reset BSTUVLO.

$$VIN \geq V_{OUT} + V_{FBOOT} + V_{BSTUV_RST} \quad (19)$$

Here, BSTUVLO reset: BSTUVLO reset voltage,
VF: the diode forward bias voltage between VIN and BST
Considering the fluctuation of BSTUVLO reset voltage and V_{FBOOT} , maximum voltage is less than 5 V.
Therefore maximum output voltage is defined as $VIN - 5 V$.

2. Restriction by Max Duty Cycle

Maximum output voltage is restricted by Max Duty Cycle (Min 85 %). In this time it is needed to consider the effect of NchFET Ron, OUTPUT current and forward voltage of SBD. OUTPUT voltage can be calculated using the following formula.

$$V_{OUT_MAX} = (VIN - R_{ONH} \times I_{OUT}) \times 0.85 - V_F \times 0.15 \quad (20)$$

Therefore maximum output voltage is defined as $VIN \times 0.7$.

Considering above restriction, adopt the lower voltage as maximum output voltage.

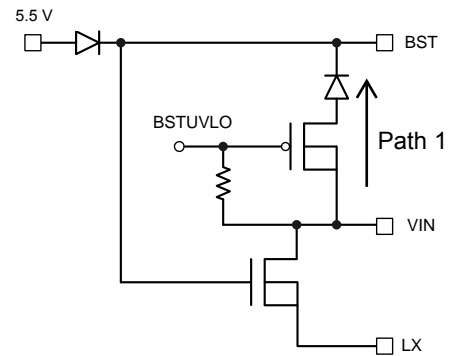


Figure 23. BST charge pass

Cautions on PCB Layout

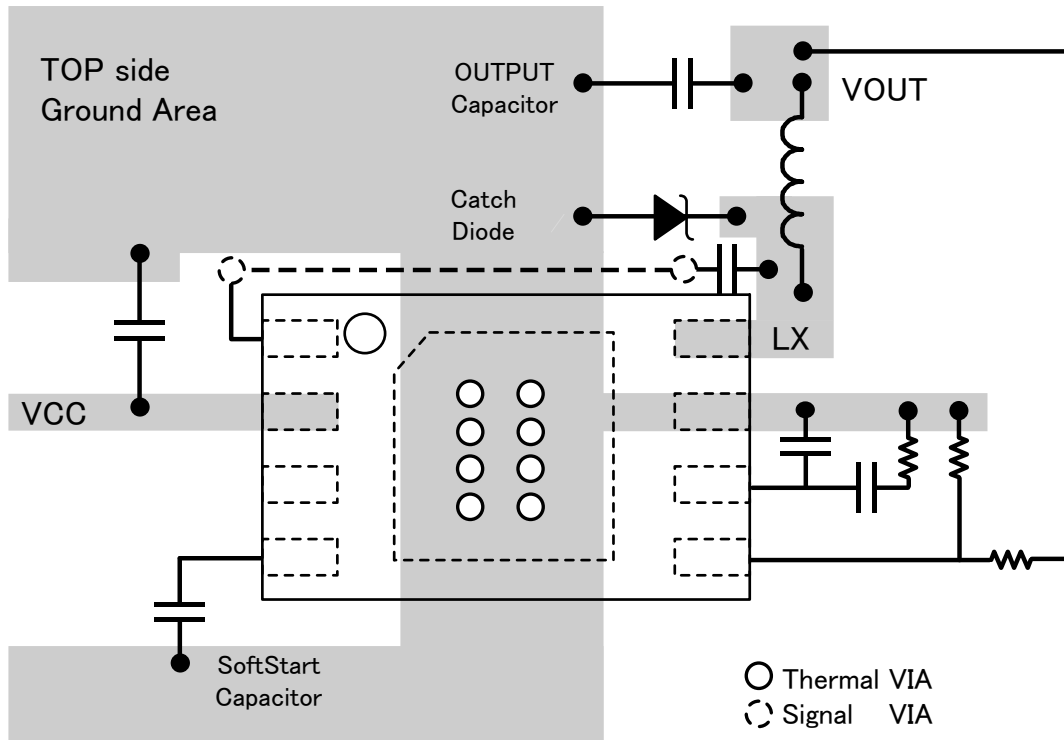


Figure 24. Reference PCB layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode.

In the BD9E151ANUX, since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. And GND area should not be connected directly power GND, connected avoiding the high current switch paths. The additional external components can be placed approximately as shown.

Power Dissipation Estimation

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.

- 1) Conduction loss : $P_{ON} = I_{OUT}^2 \times R_{ONH} \times V_{OUT} / V_{IN}$
- 2) Switching loss : $P_{SW} = 0.25 \times 10^{-9} \times V_{IN} \times I_{OUT} \times f_{SW}$
- 3) Gate charge loss : $P_G = 22.8 \times 10^{-9} \times f_{SW}$
- 4) Quiescent current loss : $P_{IC} = 0.7 \times 10^{-3} \times V_{IN}$

I_{OUT} is the output current (A), R_{ONH} is the on-resistance of the high-side MOSFET (Ω), V_{OUT} is the output voltage (V), V_{IN} is the input voltage (V), f_{sw} is the switching frequency (Hz).

Device power dissipation of IC (P) is the sum of above dissipation and estimated by following formula.

$$P = P_{ON} + P_{SW} + P_G + P_{IC}$$

Junction temperature (T_j) is estimated by following formula.

$$T_j = T_a + \theta_{ja} \times P$$

θ_{ja} is the thermal resistance of the package ($^{\circ}\text{C}$).

Please consider thermal design with sufficient margin not to over $T_{jmax} = 150^{\circ}\text{C}$.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Equivalent Circuit	Pin No.	Pin Name	Pin Equivalent Circuit
1	BST		5	FB	
2	VIN				
7	GND				
8	LX				
3	EN		6	VC	
4	SS				

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

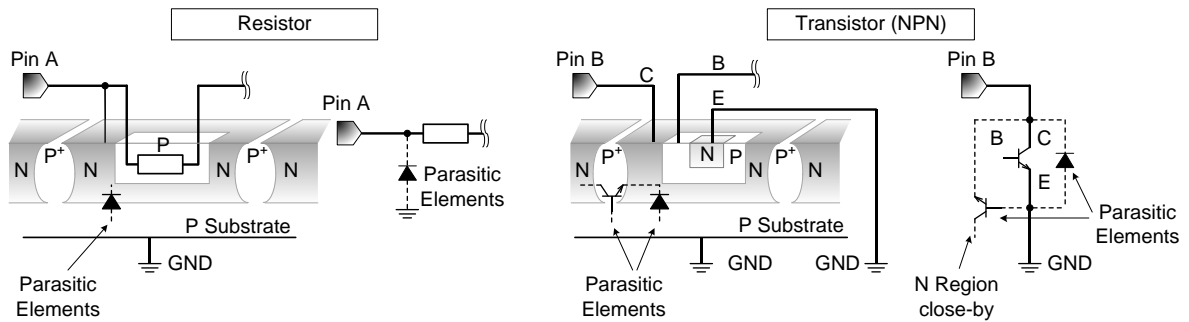


Figure 25. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

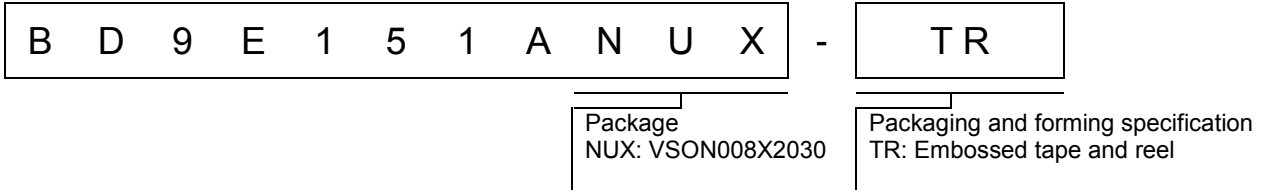
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

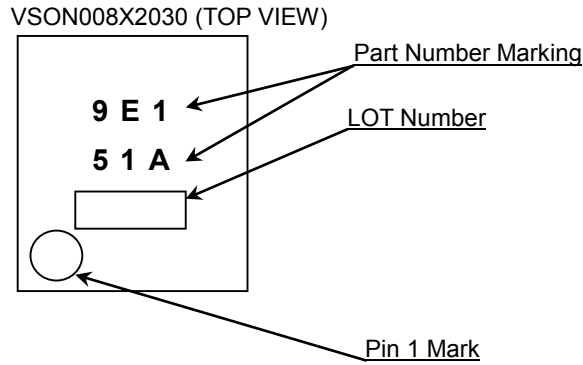
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

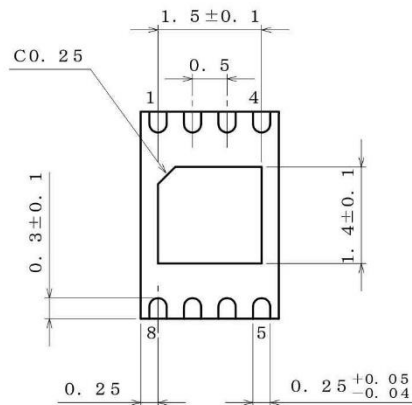
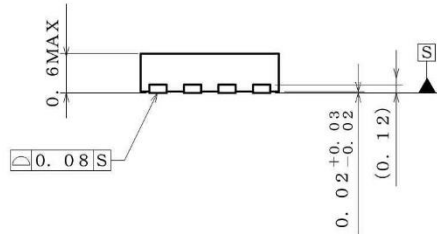
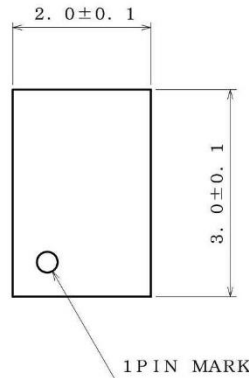


Marking Diagram



Physical Dimension and Packing Information

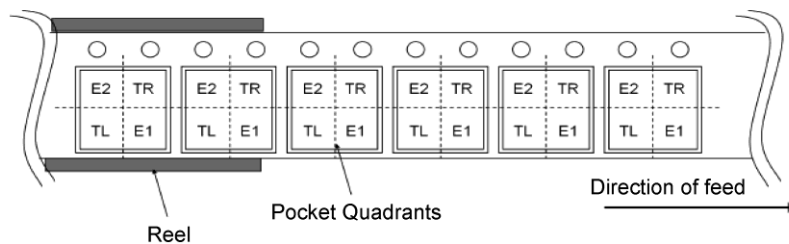
Package Name	VSON008X2030
--------------	--------------



(UNIT : mm)
 PKG : VSON008X2030
 Drawing No. EX187-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
25.Mar.2020	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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