

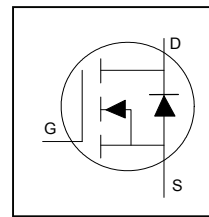
# IR MOSFET - StrongIRFET™

## Applications

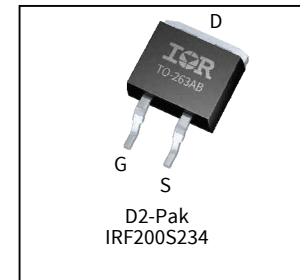
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

## Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Pb-Free ; RoHS Compliant ; Halogen-Free



<b>V<sub>DSS</sub></b>	<b>200V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>14mΩ</b>
	<b>max</b>
<b>I<sub>D</sub></b>	<b>90A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source



Halogen-Free



RoHS

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF200S234	D2-PAK	Tape and Reel	800	IRF200S234

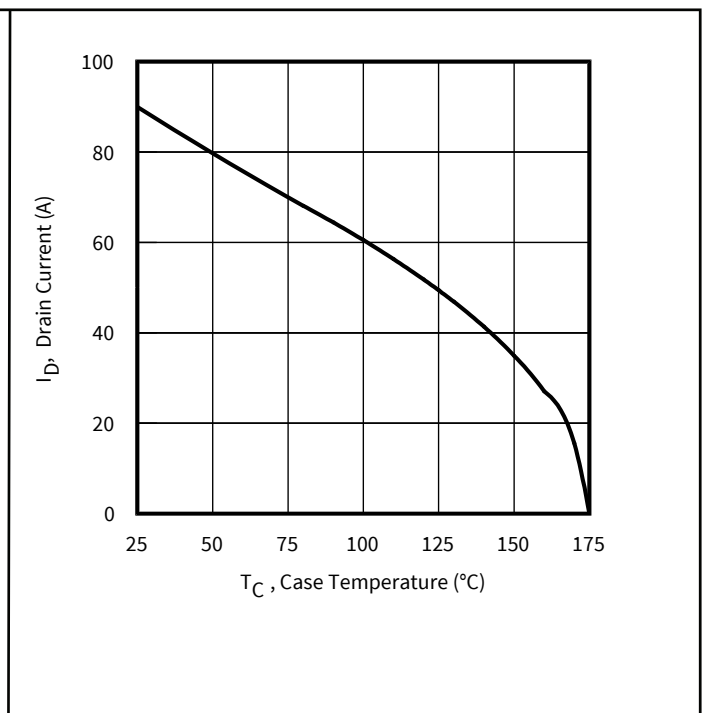
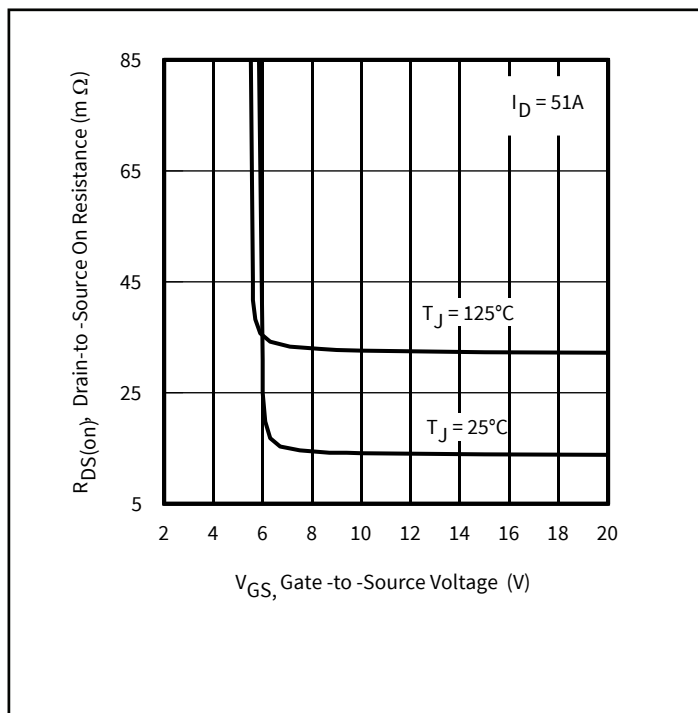


Figure 1 Typical On-Resistance vs. Gate Voltage

Figure 2 Maximum Drain Current vs. Case Temperature

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## 1 Parameters

**Table1** Key performance parameters

Parameter	Values	Units
$V_{DS}$	200	V
$R_{DS(on) \max}$	16.9	m $\Omega$
$I_D$	90	A

## 2 Maximum ratings and thermal characteristics

**Table 2 Maximum ratings (at  $T_J=25^\circ\text{C}$ , unless otherwise specified)**

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$ , $V_{GS} @ 10\text{V}$	90	A
Continuous Drain Current	$I_D$	$T_C = 100^\circ\text{C}$ , $V_{GS} @ 10\text{V}$	61	
Pulsed Drain Current ①	$I_{DM}$	$T_C = 25^\circ\text{C}$	312	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	417	W
Linear Derating Factor		$T_C = 25^\circ\text{C}$	2.8	W/ $^\circ\text{C}$
Gate-to-Source Voltage	$V_{GS}$	-	$\pm 20$	V
Operating Junction and Storage Temperature Range	$T_J$ $T_{STG}$	-	-55 to + 175	$^\circ\text{C}$
Soldering Temperature, for 10 seconds (1.6mm from case)	-	-	300	

**Table 3 Thermal characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case ⑦	$R_{\theta JC}$	$T_J$ approximately $90^\circ\text{C}$	-	-	0.36	$^\circ\text{C}/\text{W}$
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	-	-	0.50	-	
Junction-to-Ambient ⑧	$R_{\theta JA}$	(PCB Mount) (D2-Pak)	-	-	40	

**Table 4 Avalanche characteristics**

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	$E_{AS}$ (Thermally limited)	574	mJ
Single Pulse Avalanche Energy ⑨	$E_{AS}$ (Thermally limited)	693	
Avalanche Current ①	$I_{AR}$	See Fig 16, 17, 23a, 23b	A
Repetitive Avalanche Energy ①	$E_{AR}$		mJ

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.436\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 51\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 51\text{A}$ ,  $di/dt \leq 1899\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.:
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 37\text{A}$ ,  $V_{GS} = 10\text{V}$

### 3 Electrical characteristics

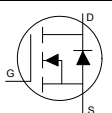
**Table 5 Static characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	200	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, $I_D = 3.0mA$ ①	-	0.18	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 51A$	-	14	16.9	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	3.0	-	5.0	V
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{DS} = 200V, V_{GS} = 0V$	-	-	20	μA
		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ C$	-	-	250	
Gate-to-Source Forward Leakage	$I_{GSS}$	$V_{GS} = 20V$	-	-	100	nA
Gate-to-Source Reverse Leakage	$I_{GSS}$	$V_{GS} = -20V$	-	-	-100	nA
Gate Resistance	$R_G$		-	2.4	-	Ω

**Table 6 Dynamic characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	$V_{DS} = 50V, I_D = 51A$	96	-	-	S
Total Gate Charge	$Q_g$	$I_D = 51A$ $V_{DS} = 100V$ $V_{GS} = 10V$	-	108	162	nC
Gate-to-Source Charge	$Q_{gs}$		-	26	-	
Gate-to-Drain Charge	$Q_{gd}$		-	37	-	
Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	$Q_{sync}$		-	71	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100V$	-	21	-	ns
Rise Time	$t_r$	$I_D = 51A$	-	58	-	
Turn-Off Delay Time	$t_{d(off)}$	$R_G = 2.7\Omega$	-	67	-	
Fall Time	$t_f$	$V_{GS} = 10V$	-	37	-	
Input Capacitance	$C_{iss}$	$V_{GS} = 0V$	-	6484	-	pF
Output Capacitance	$C_{oss}$	$V_{DS} = 50V$	-	462	-	
Reverse Transfer Capacitance	$C_{rss}$	$f = 1.0MHz$ , See Fig.7	-	142	-	
Effective Output Capacitance (Energy Related)	$C_{oss\ eff.(ER)}$	$V_{GS} = 0V, V_{DS} = 0V$ to 160V ⑥	-	356	-	
Output Capacitance (Time Related)	$C_{oss\ eff.(TR)}$	$V_{GS} = 0V, V_{DS} = 0V$ to 160V ⑤	-	491	-	

**Table 7 Reverse Diode**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	90	A
Pulsed Source Current (Body Diode) ①	$I_{SM}$		-	-	312	
Diode Forward Voltage	$V_{SD}$	$T_J = 25^\circ C, I_S = 51A, V_{GS} = 0V$ ④	-	-	1.3	V
Peak Diode Recovery $dv/dt$ ③	$dv/dt$	$T_J = 175^\circ C, I_S = 51A, V_{DS} = 200V$	-	26	-	V/ns
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C$ $V_{DD} = 170V$	-	117	-	ns
		$T_J = 125^\circ C$ $I_F = 51A,$	-	140	-	
Reverse Recovery Charge	$Q_{rr}$	$T_J = 25^\circ C$ $di/dt = 100A/\mu s$ ④	-	563	-	nC
		$T_J = 125^\circ C$	-	801	-	
Reverse Recovery Current	$I_{RRM}$	$T_J = 25^\circ C$	-	8.7	-	A

### 4 Electrical characteristic diagrams

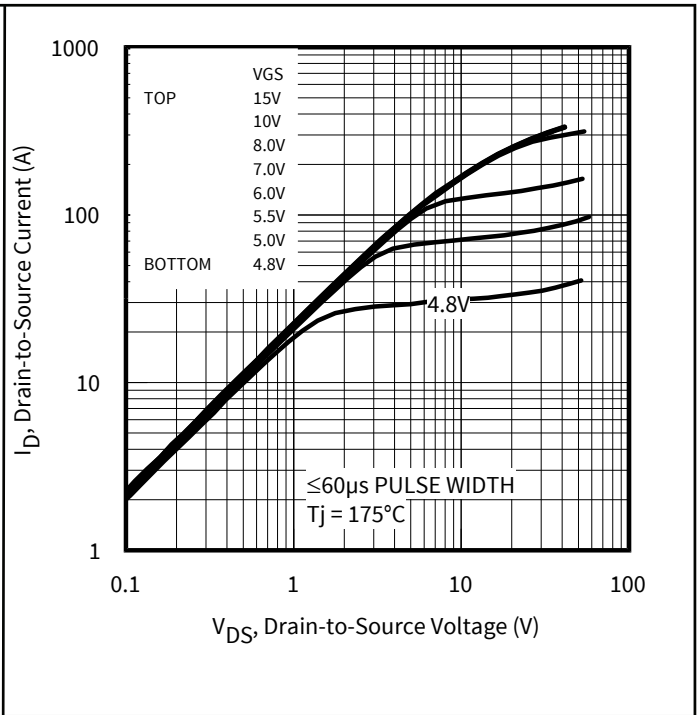
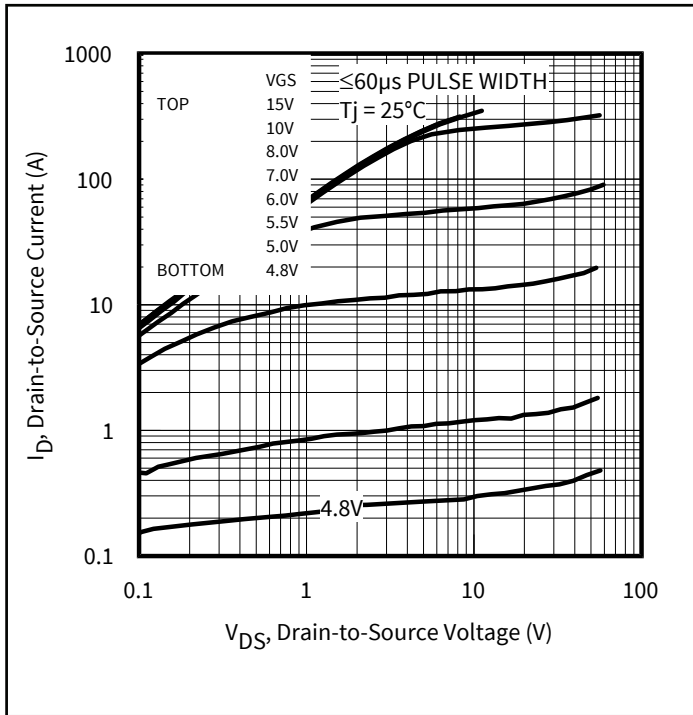


Figure 3 Typical Output Characteristics

Figure 4 Typical Output Characteristics

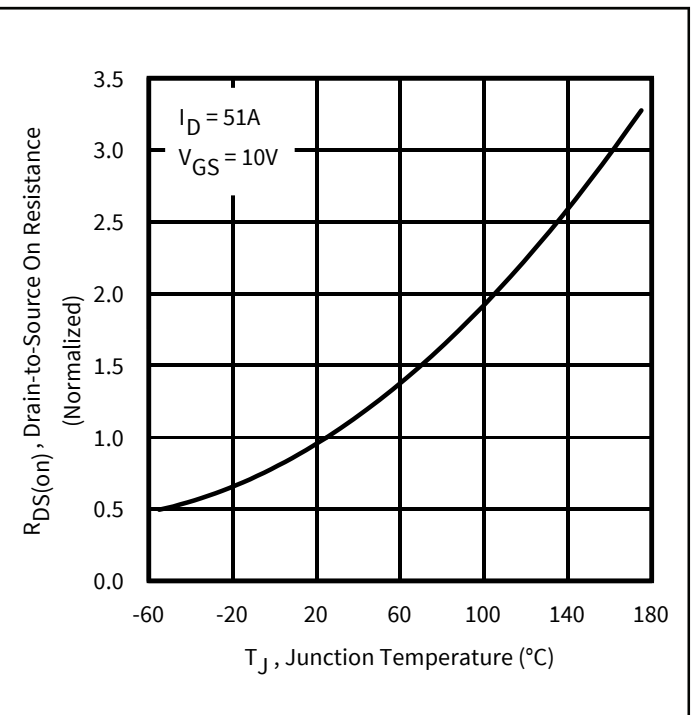
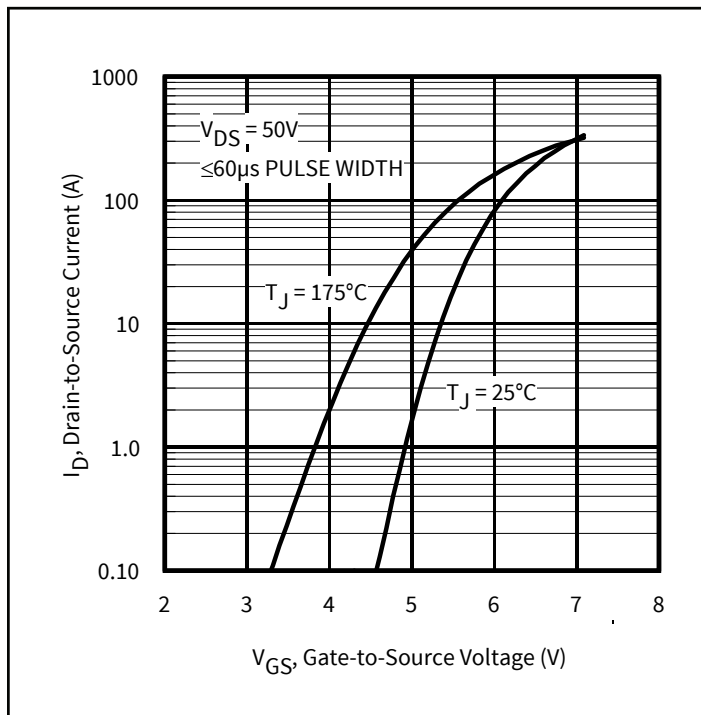
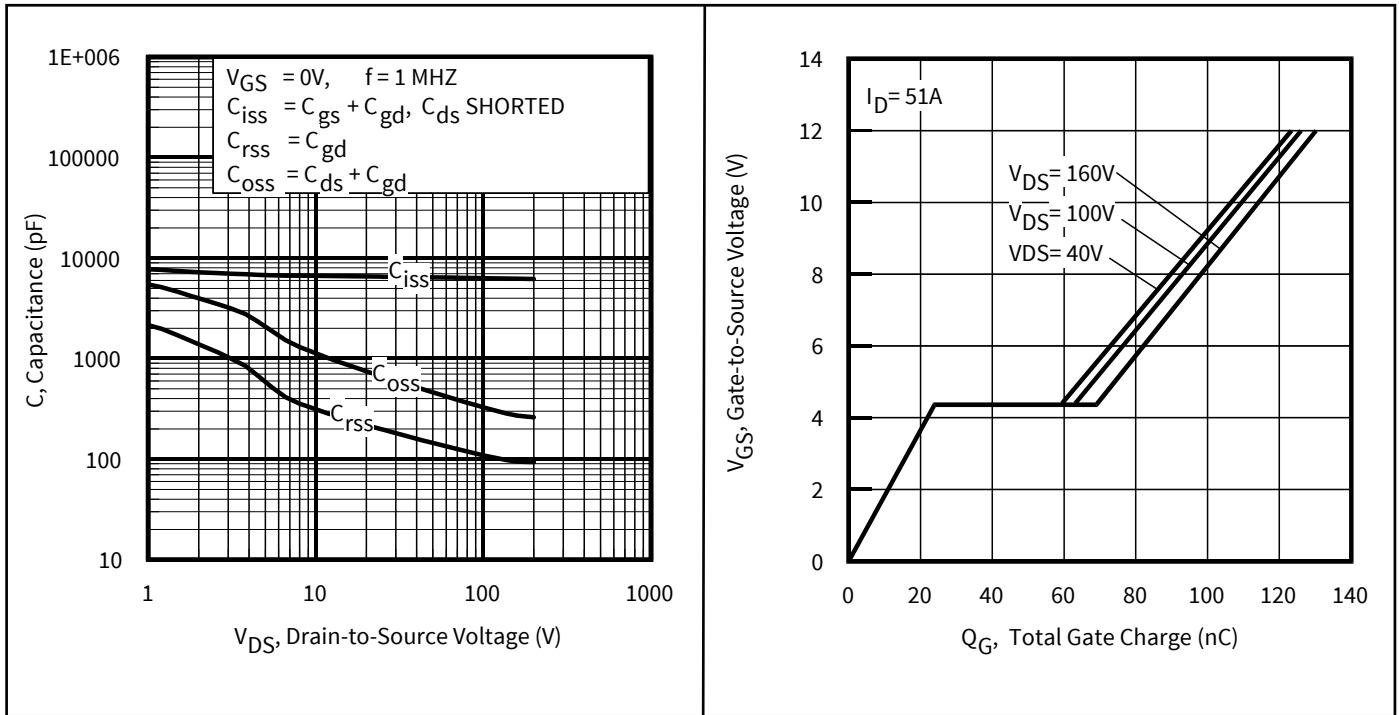


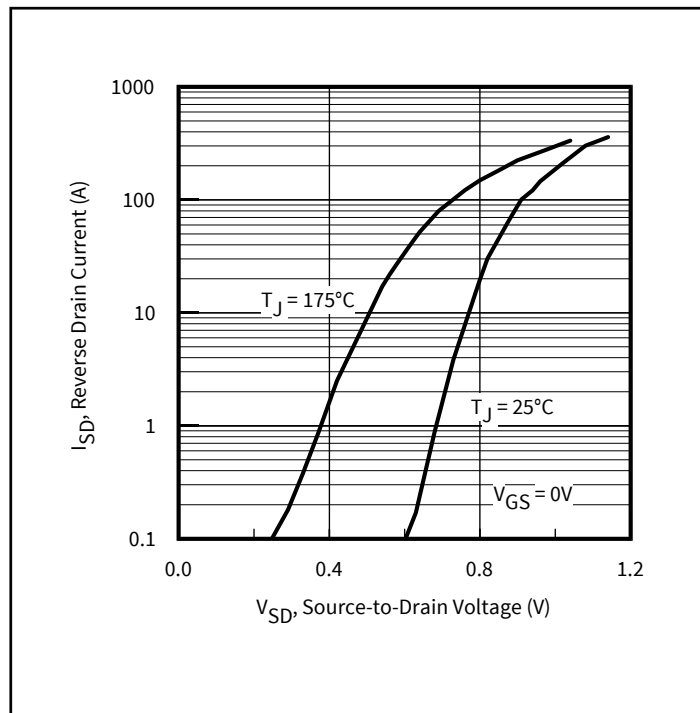
Figure 5 Typical Transfer Characteristics

Figure 6 Normalized On-Resistance vs. Temperature



**Figure 7 Typical Capacitance vs. Drain-to-Source Voltage**

**Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage**



**Figure 9 Typical Source-Drain Diode Forward Voltage**

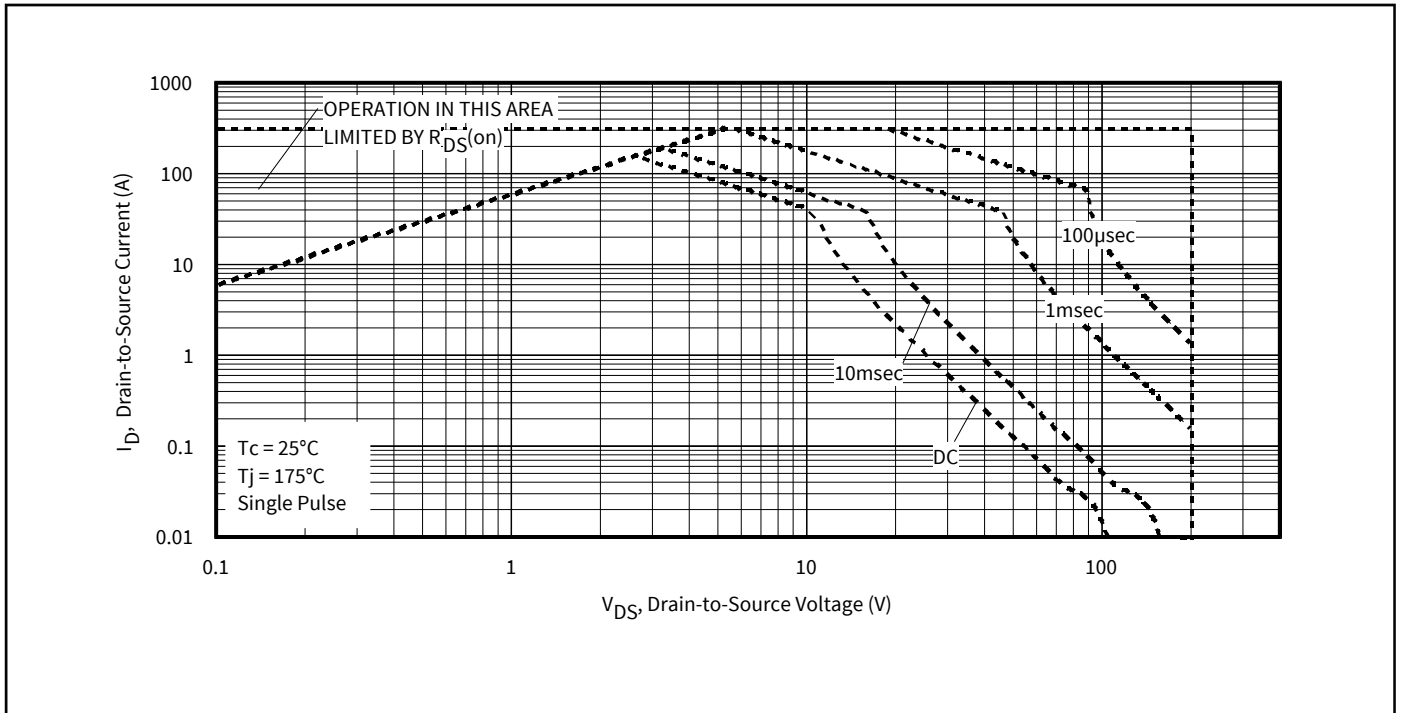


Figure 10 Maximum Safe Operating Area

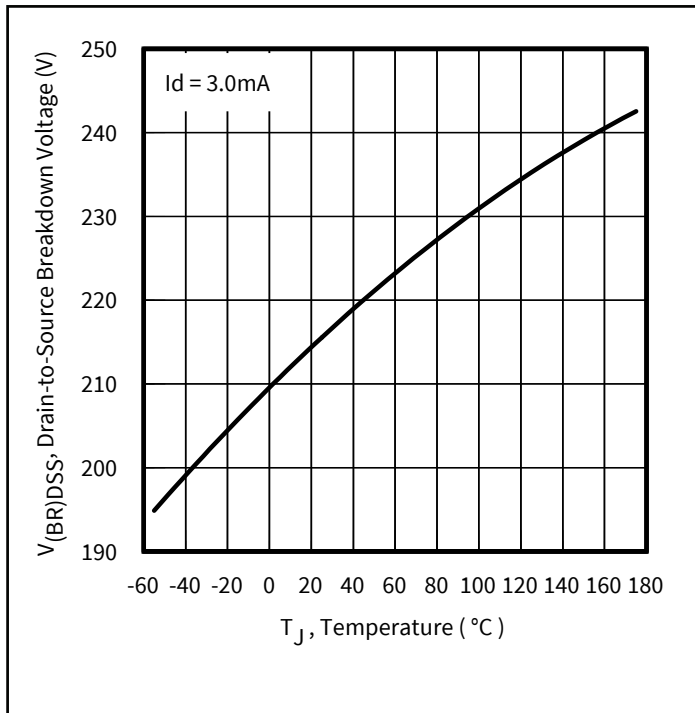


Figure 11 Drain-to-Source Breakdown Voltage

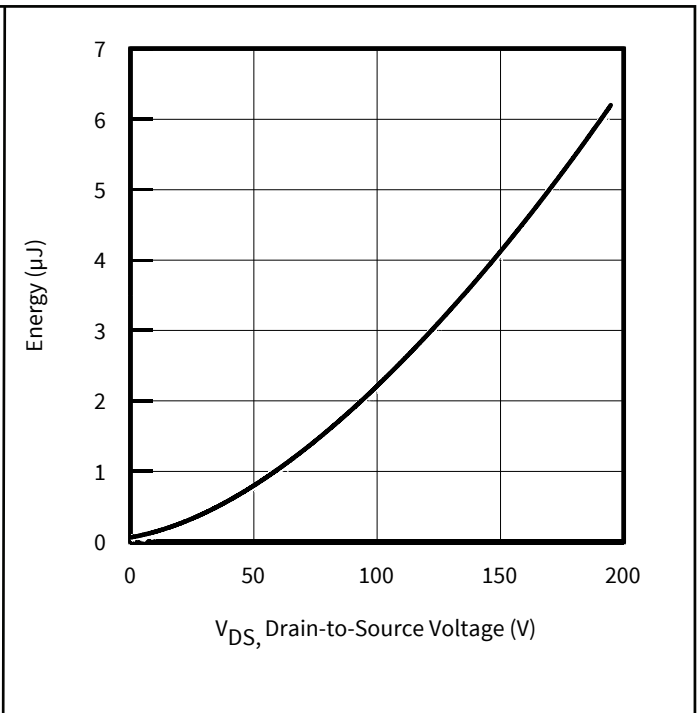


Figure 12 Typical Coss Stored Energy



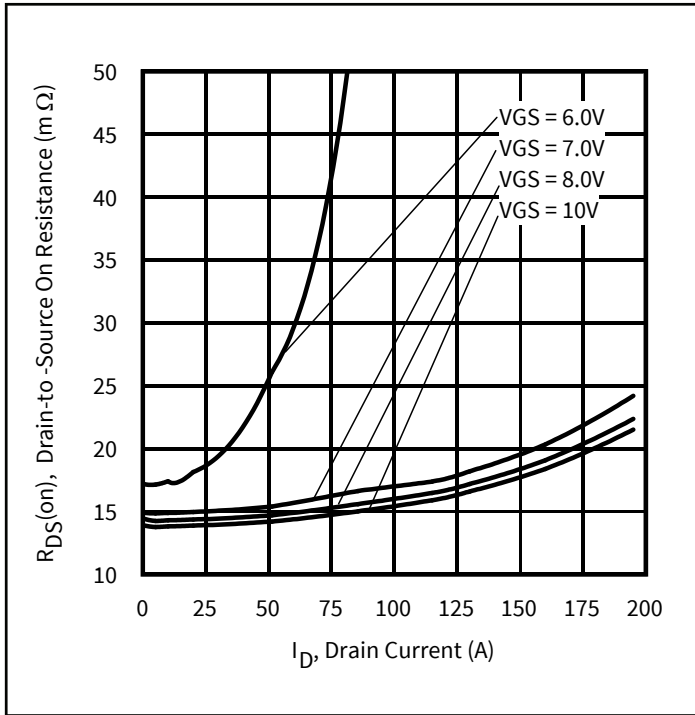


Figure 13 Typical On-Resistance vs. Drain Current

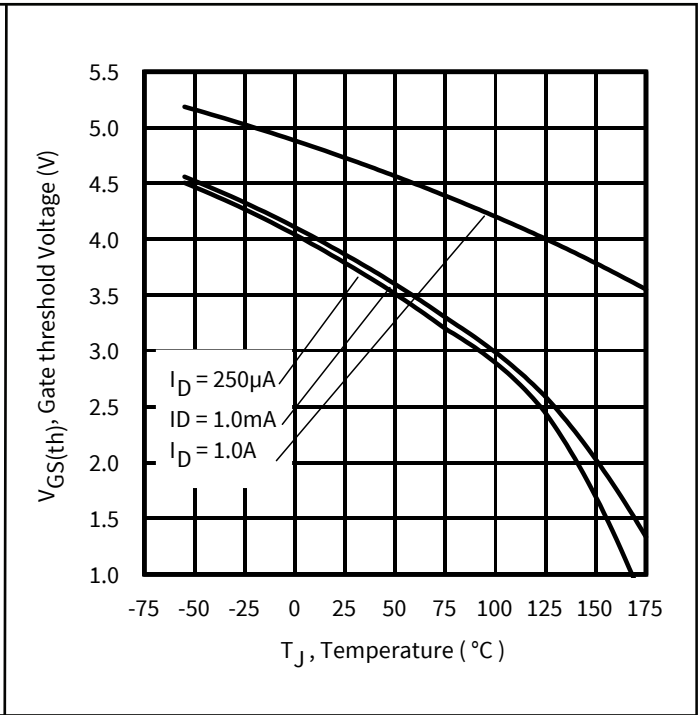


Figure 14 Threshold Voltage vs. Temperature

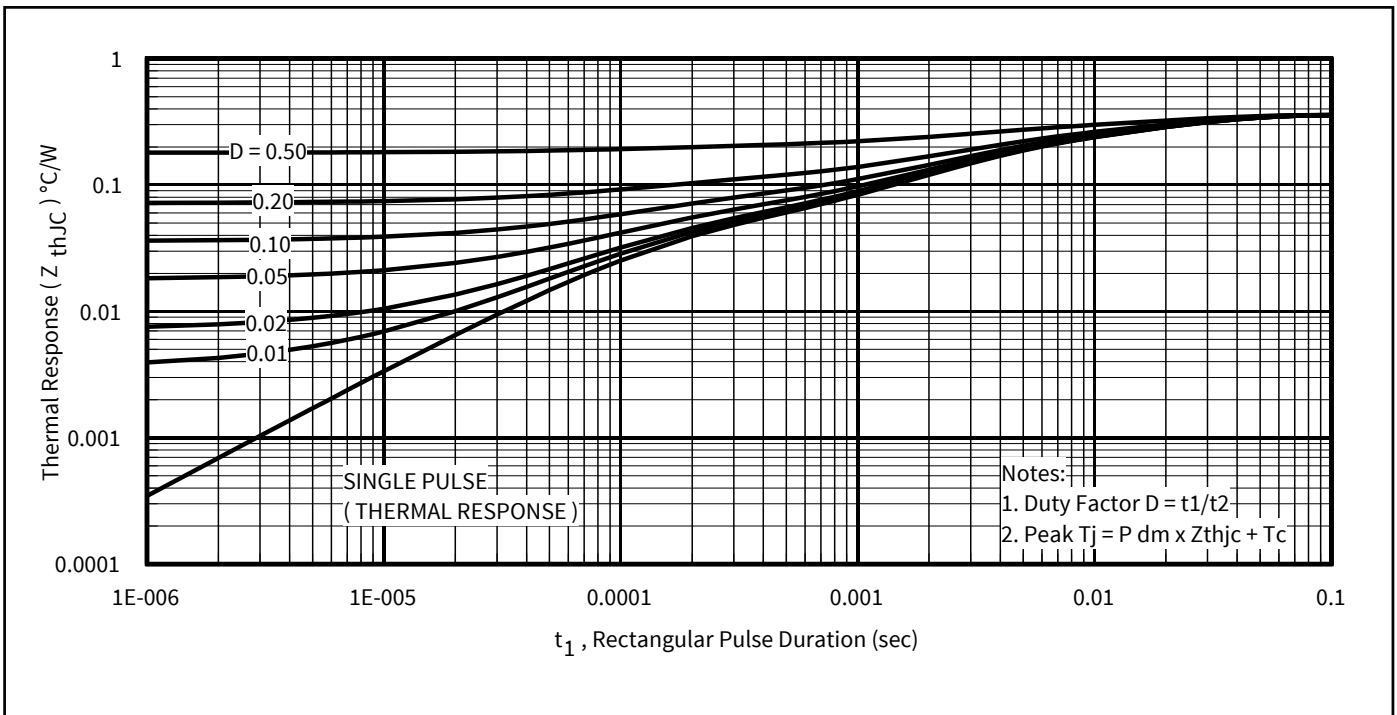


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

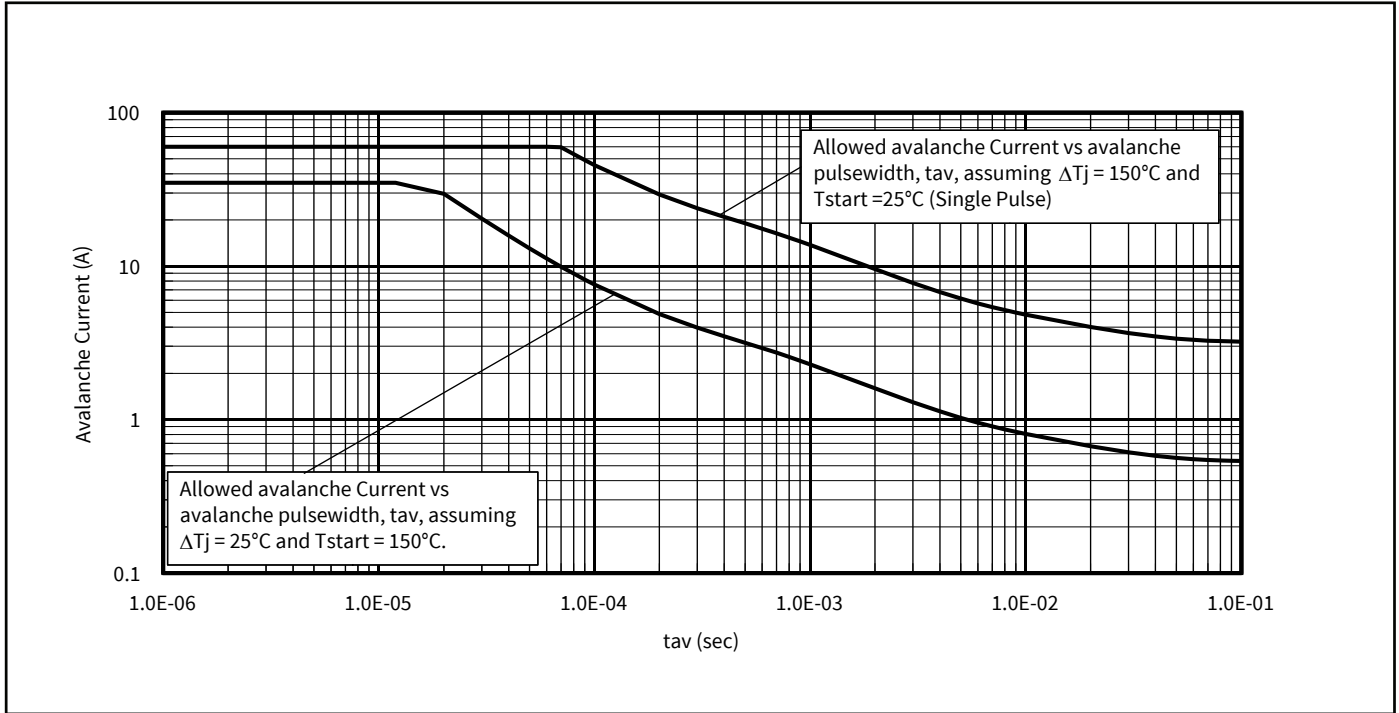
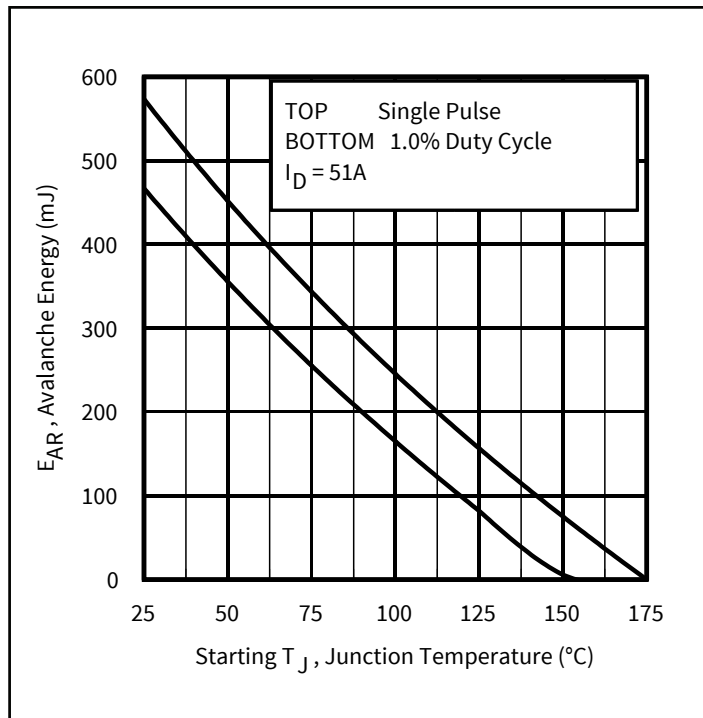


Figure 16 Avalanche Current vs. Pulse Width



**Notes on Repetitive Avalanche Curves , Figures 16, 17:  
(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7. DT = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)  
 $PD(ave) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

Figure 17 Maximum Avalanche Energy vs. Temperature

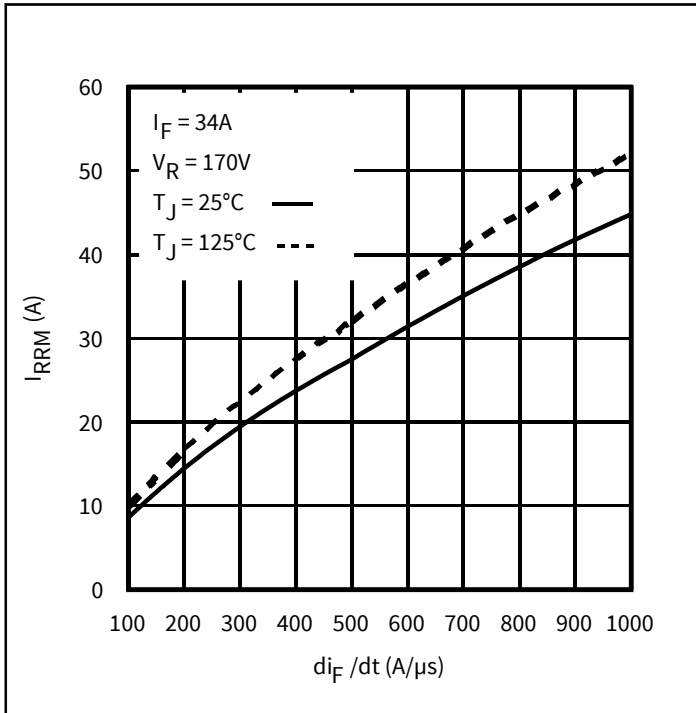


Figure 18 Typical Recovery Current vs.  $di_F/dt$

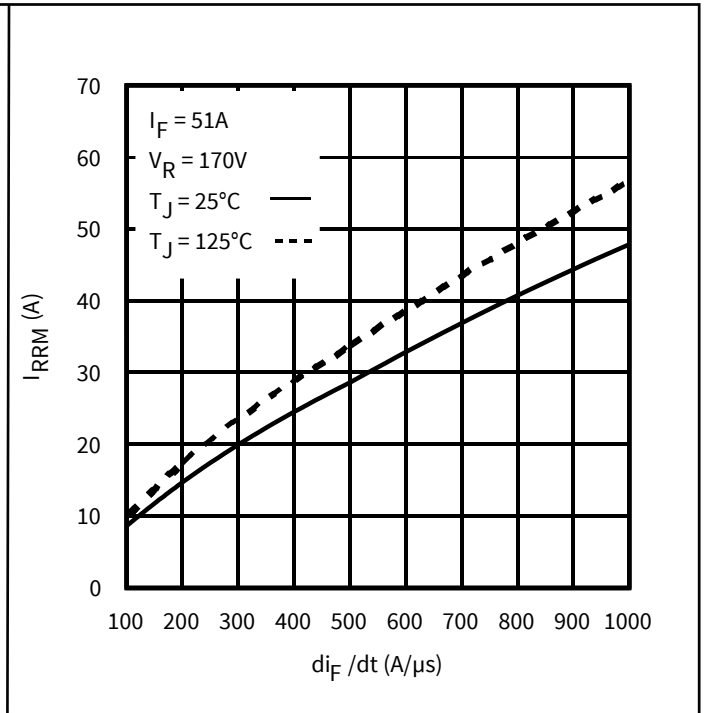


Figure 19 Typical Recovery Current vs.  $di_F/dt$

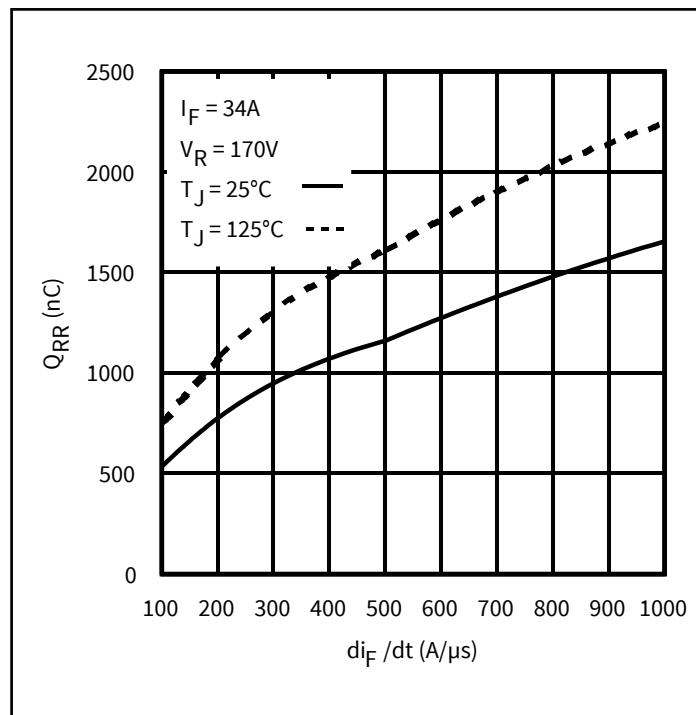


Figure 20 Typical Stored Charge vs.  $di_F/dt$

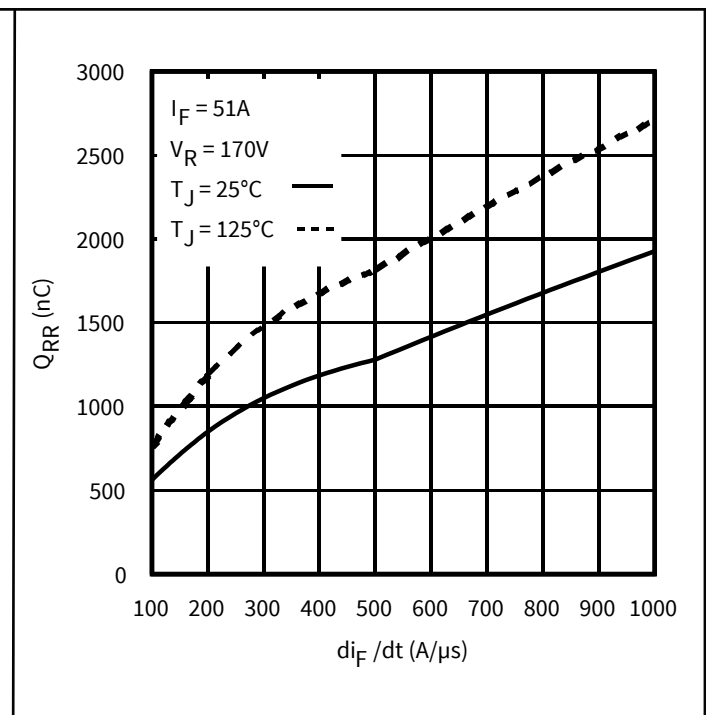


Figure 21 Typical Stored Charge vs.  $di_F/dt$

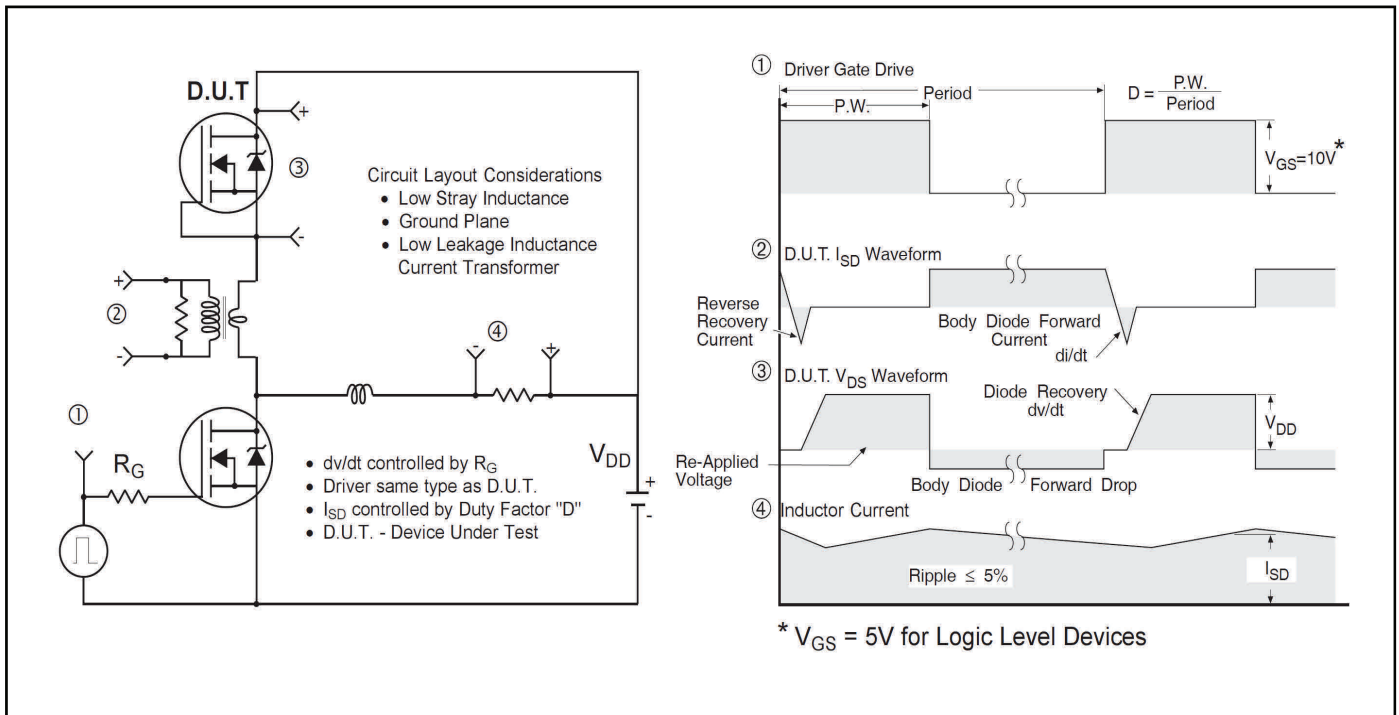


Figure 22 Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel Power MOSFETs

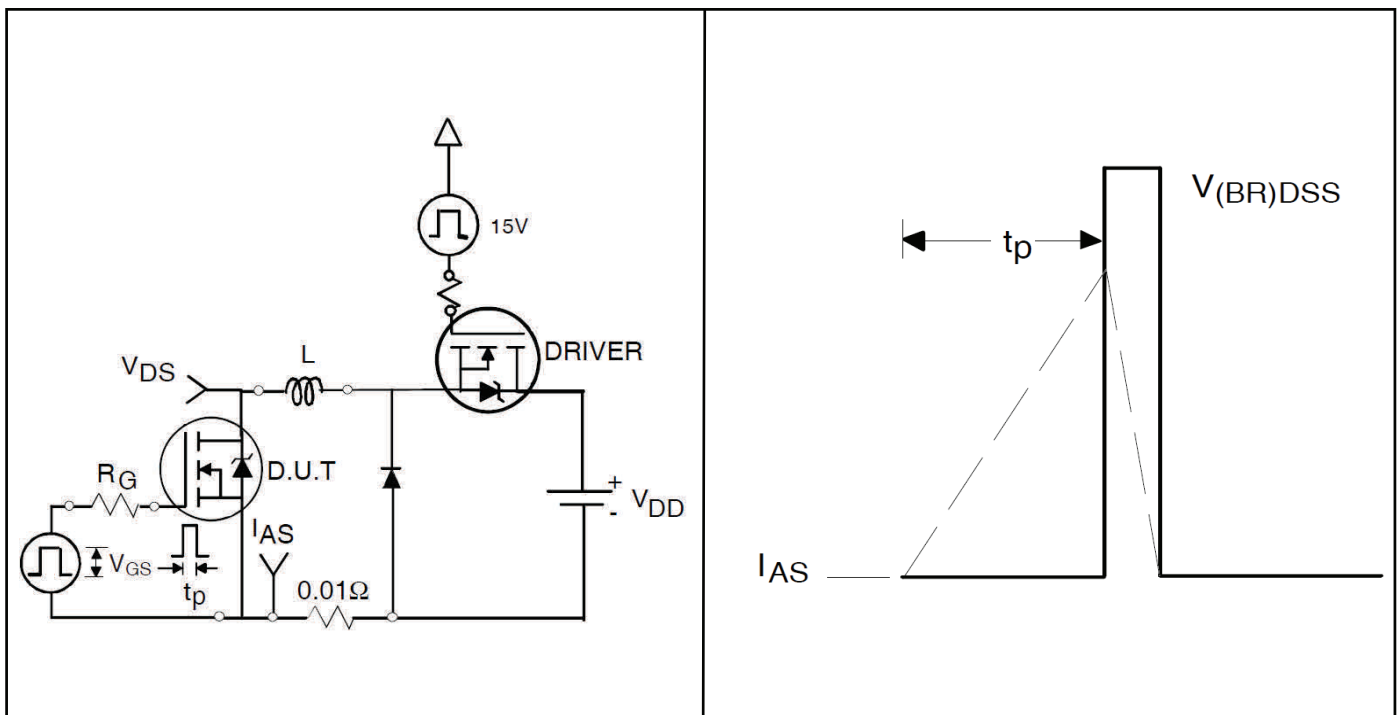


Figure 23a Unclamped Inductive Test Circuit

Figure 23b Unclamped Inductive Waveforms

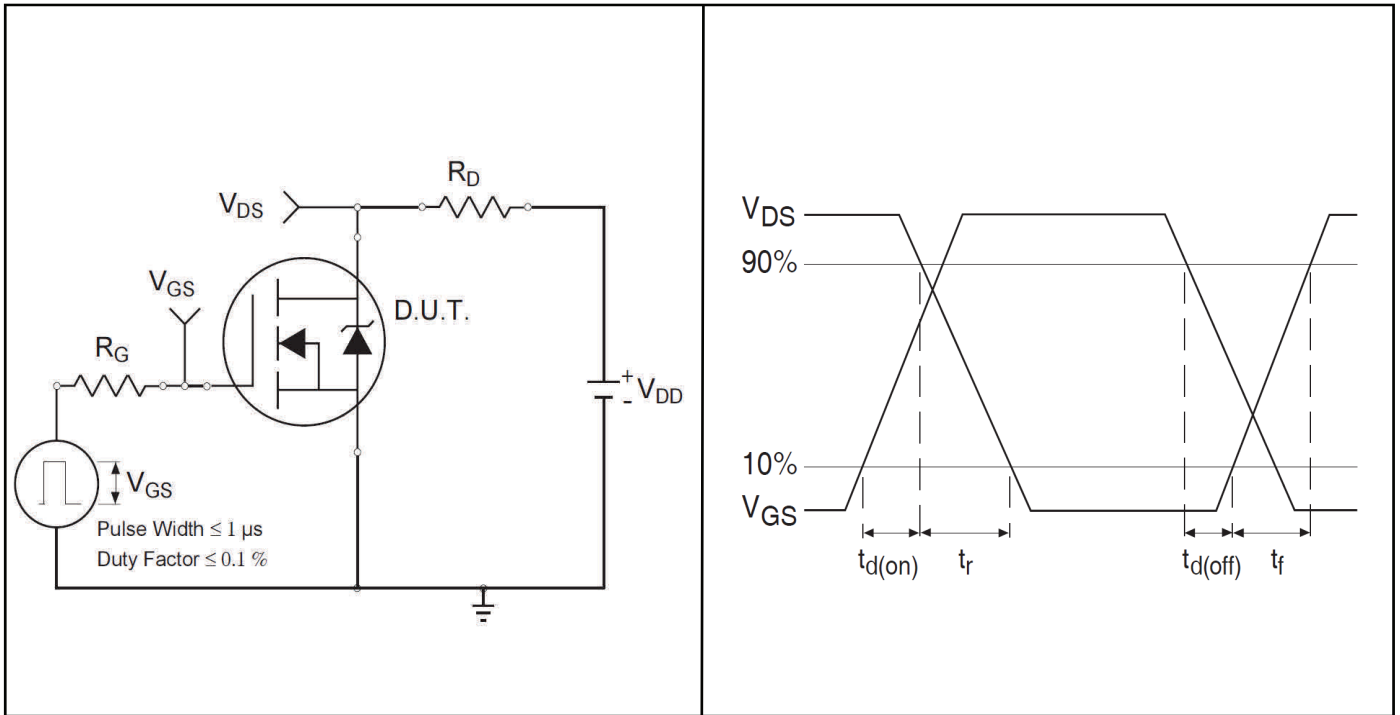


Figure 24a Switching Time Test Circuit

Figure 24b Switching Time Waveforms

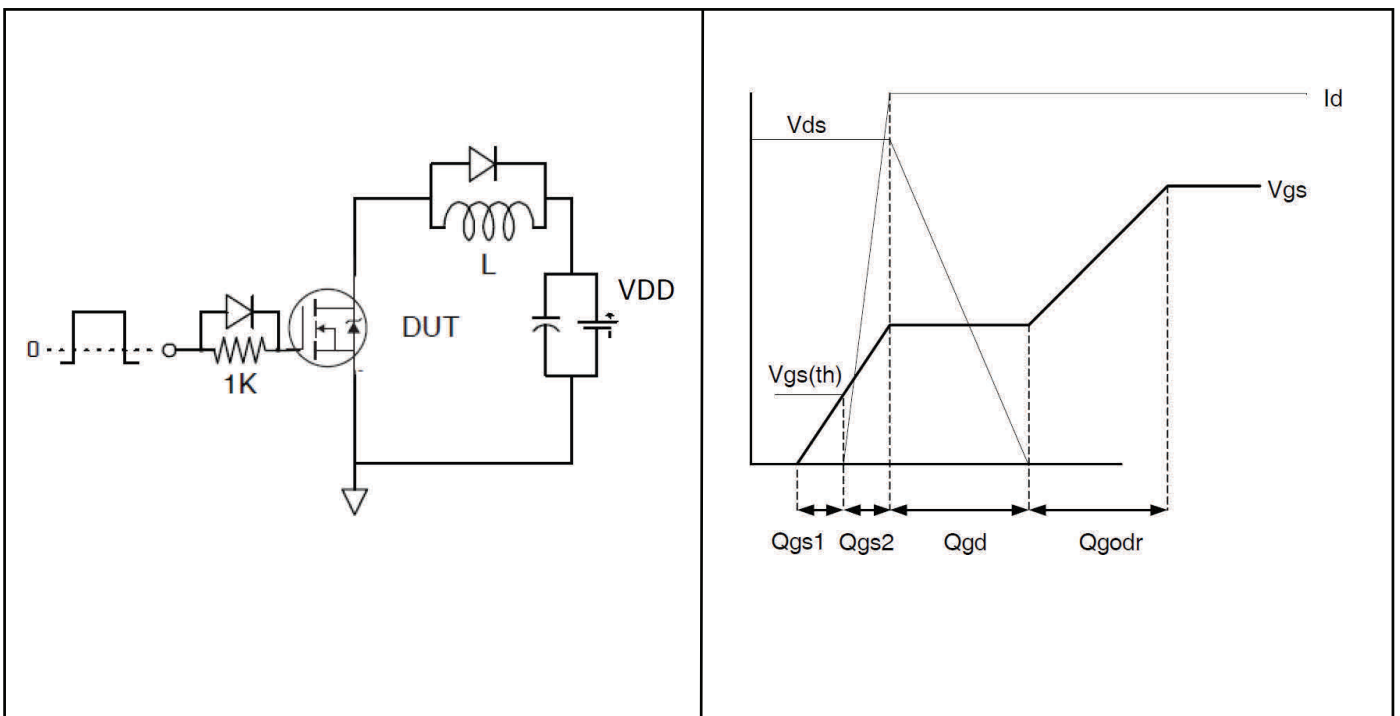
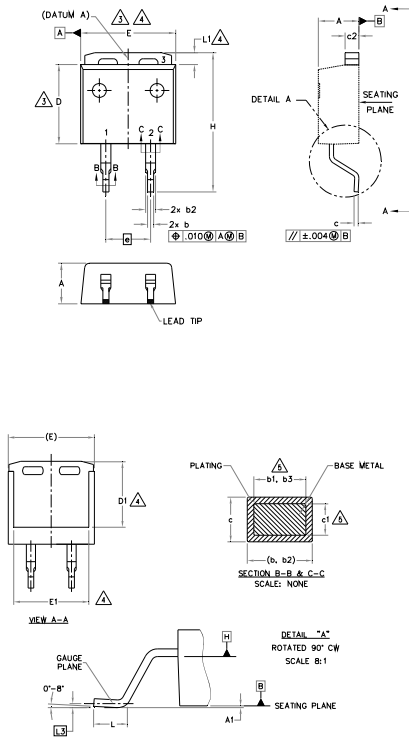


Figure 25a Gate Charge Test Circuit

Figure 25b Gate Charge Waveform

## 5 Package Information

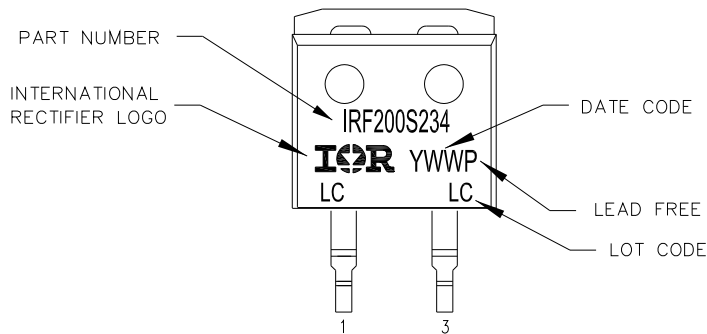
### D2Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	NOTES: 1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES] 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H. 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1. 5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY. 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H. 7. CONTROLLING DIMENSION: INCH. 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB EXCEPT FOR DIM E1.
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	8.00	9.00	.315	.354	
e	5.08 BSC		.200 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L3	0.25 BSC		.010 BSC		

- NOTES:  
 1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994  
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]  
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.  
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.  
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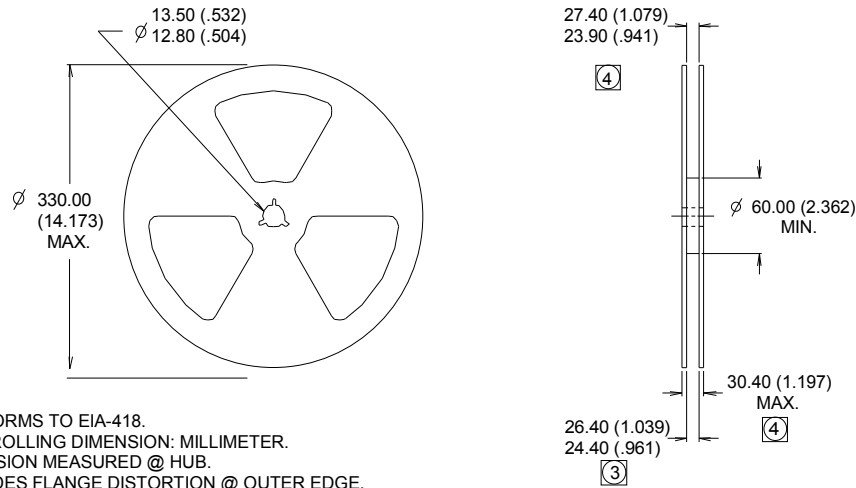
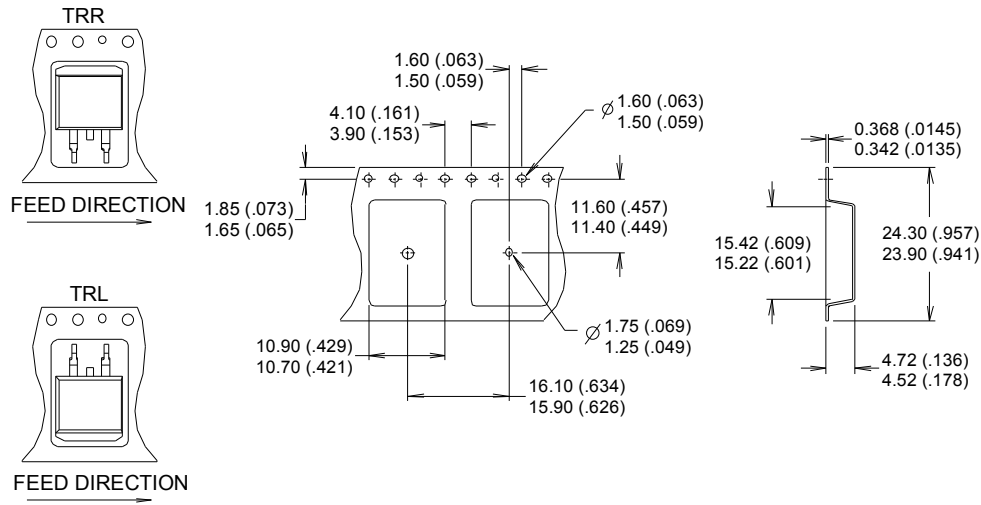
### D2Pak (TO-263AB) Part Marking Information



TOP MARKING (LASER)

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

**D2Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))



- NOTES :
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

## 6 Qualification Information

### Qualification Information

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) †	
<b>Moisture Sensitivity Level</b>	D2Pak	MSL1 (per JEDEC J-STD-020D†)
<b>RoHS Compliant</b>	Yes	

† Applicable version of JEDEC standard at the time of product release.



**Revision History****Major changes since the last revision**

<b>Page or Reference</b>	<b>Revision</b>	<b>Date</b>	<b>Description of changes</b>
All pages	1.0	2016-09-23	• First release Provisional data sheet.
All pages	2.0	2017-06-30	• First release Final data sheet.

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**Edition 2015-05-06**  
**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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