NCL2801LED1GEVB

NCL2801LED1 High Precision 200 W Power Factor Controller Evaluation Board User's Manual

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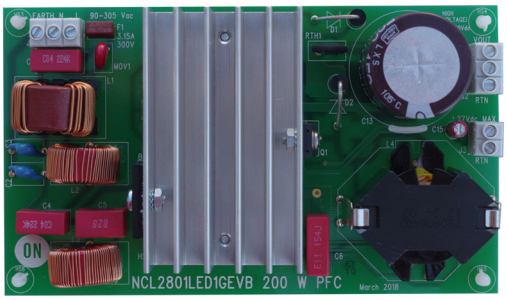
EVAL BOARD USER'S MANUAL



Evaluation Board Overview

This manual covers the specification, construction, and testing of the NCL2801 evaluation board. This board is configured as a 200 W Power Factor Corrector front end suitable for conditioning the input power of various switch−mode power supplies. This board provides high power factor and low total harmonic distortion of input current over the extended input voltage range and very wide output load range. Performance exceeds requirements for many demanding applications including LED lighting, computing power, and white goods products.

The Key Features of this Demo Board

- Very Low THDi Across a Wide Operating Range
- High Power Factor
- Fast Response to Dynamic Loading
- Valley Count Frequency Foldback Improves Efficiency
- Tight Output Voltage Regulation
- Two Levels of Over Voltage Protection
- Brown Out/In Protection
- Line Feedforward
- Current Limit
- Open/Short Pin Protection

Table 1. SPECIFICATIONS

Input Voltage	100 – 277	V ac
Line Frequency	50/60	Hz
THDi (>30% Load)	10%	Max.
Power Factor (>30% Load)	0.9	Min.
Output Voltage	450 ±4%	V dc
Output Power	200	W typ.
Efficiency (>30% Load, 230 V ac)	95%	Min.
Ripple	10.5	Vpk – Pk

THEORY OF OPERATION

The NCL2801 is designed to control high power factor boost converters. General information on boost converter operation can be found in other literature. This description will focus on aspects which have been optimized to provide very low THDi and high efficiency.

The circuit operates in Critical Conduction Mode (CrM) for high loads, and transitions to Discontinuous Mode at lighter loads by forcing a dead time. This innovative Valley Count Frequency Fold−back method reduces the switching frequency while preserving the benefits of traditional CrM operation. The start of the next switching cycle is timed to the power MOSFET drain voltage ringing after the end of demagnetization which improves efficiency by switching at the valley. Internal circuity allows near−unity power factor even when the switching frequency is reduced. Introducing delay lowers the switching frequency and can improve efficiency under certain load conditions.

Unlike typical CrM boost converters based on voltage mode control, the NCL2801 utilizes current mode control providing more precise operation. A multiplier is required to condition the envelope of the input current waveform. This IC features a novel multiplier design to deliver very low input current THDi over a broad power range.

An offset is introduced to the output of the multiplier to compensate for non−ideal nature of the process. This function maintains sinusoidal input current waveform especially near the zero crossings of the applied input.

Line Feedforward compensation adjusts the gain of the controller to improve wide range control. Gain is reduced at high input voltage and increased when the applied voltage drops to a lower level. This gain change maintains the output of the error amplifier, or VCTR, in a more desirable operating range away from low level noise and high level clipping. The gain change occurs in the unused input voltage band between 150 and 180 V ac. The change is clearly visible by monitoring VCTR while applied voltage passes through this range. Range change has no effect while operating in typical global mains voltage ranges.

High power factor converters use low loop bandwidth to maintain high PF and low THDi performance. As such, response to input voltage or output load changes is typically slow and suffers large deviation from the regulated value. The NCL2801 features a Dynamic Response Enhancer (DRE) which quickly restores the control loop to the required range in response to changes in power. DRE maintains the output voltage even during an extreme zero to 100% load change. The DRE function is also active during initial startup to speed the process of charging the output capacitor. This DRE function allows use of smaller and lower cost output capacitors in place of larger values often used to mitigate the effects of load changes.

Two Over Voltage Protection (OVP) functions are included in this version of NCL2801. The first OVP activates at 105% of nominal output voltage and gradually reduces on−time to zero. This reduces the power processing gradually over a period of time avoiding erratic control of the output voltage. This function typically manages events like rapid changes in applied voltage or load. If the output voltage continues to rise to 107% of nominal, a second OVP function stops all switching to avoid a run−away situation. Switching resumes when the output voltage returns to normal. The OVP functions can be observed during initial startup and for large reductions in output load.

The CS pin links the switch current to the boost control function. This pin also provides over current protection on a cycle by cycle basis. A programming feature is also managed by the CS pin. At initial power up, the NCL2801 outputs a current through the CS pin to read a resistor placed on the circuit board. A lookup table links the measured resistance to one of six levels. Resistance below 50 Ω nominal is interpreted as a shorted pin, or assembly fault which stops the converter from operating. Nominal impedances of 150, 330, 620, and 1 kΩ are linked to one of four thresholds determining when the control function changes from CrM to DCM operation. A resistance measurement greater than about 1.3 kΩ nominal is considered an open circuit, or assembly fault which disables the converter. This feature allows easy configuration of the operating mode and detects faults on the circuit board. This EVB is fitted with 150 Ω which invokes the lowest CrM to DCM threshold.

PIN DESCRIPTIONS

FB Pin

The feedback pin is the input for several essential functions. Each will be described in the following sections.

Voltage Regulation

The feedback pin couples a voltage from the PFC output resistor divider to the error amplifier where it is compared to the internal 2.5 V (nom) reference and creates a signal to maintain voltage regulation. A small capacitor is used to filter high frequency noise.

Under Voltage Protection

A minimum voltage is required on the FB pin before the controller will enter the active mode. This ensures integrity of the output voltage divider thus avoiding uncontrolled operation. Voltage is required to be above V_{UVPH} threshold, typically 450 mV.

Over Voltage Protection

The two levels of OVP are monitored via the feedback pin. The first level provides a gradual protection while the second prevents damage should the first level response becomes too slow. The second OVP stops DRV pulses until the output voltage returns to a nominal level.

VCTRL Pin

The transconductance error amplifier output is available on this pin.

A compensation network connected between this pin and ground controls loop bandwidth. This signal is not intended for any external control.

MULT Pin

Control Function

This pin connects to a resistor divider to receive a scaled down rectified mains voltage. A small capacitor is used to filter high frequency noise. Proper operation relies on this signal accurately representing the applied input voltage.

Line Feedforward

Input voltage is averaged and compared with a reference to set gain of the control algorithm. Line Range change dramatically improves THDi performance by optimizing the range of voltage on VCTRL.

Brown Out/In

A comparator with hysteresis monitors the input voltage via a resistor divider and inhibits operation on the EVB until the voltage exceeds ~85 V ac. If input voltage drops below ~80 V ac, DRV signals are stopped.

CS Pin

Current Mode Control

MOSFET current information enters through this pin. The control functions rely on accurate cycle by cycle current information. As such, this pin typically does not need any filtering.

CrM – DCM Threshold

When Vcc bias power is first applied, the controller monitors the voltage on the CS Pin in response to an internal current source delivering a precise current. The measured voltage identifies a resistor on the circuit board between the CS Pin and the MOSFET current sense resistor. One of four operational bins is set to determine the VCTRL voltage required to transition from CrM to DCM or Valley Count Frequency Foldback mode.

ZCD Pin

This pin senses the voltage on the auxiliary winding of the boost inductor. When zero current, or demagnetization, is achieved a new switching cycle is initiated. This signal is also utilized in Valley Count Frequency Foldback to synchronize the DRV signal to the power MOSFET drain voltage valley. Switching at local minima improves efficiency.

A series resistor between the ZCD Pin and auxiliary winding limits current through the pin.

GND

This is the ground or return reference pin for the controller.

DRV Pin

Connect the DRV pin to the gate of the MOSFET through a suitable network. Switching times can be modified via a collection of resistors and diodes to optimize operation of diode recovery and electromagnetic interference.

Vcc Pin

This pin receives the bias power for the controller. This EVB utilizes 12.5 V dc nominal start threshold.

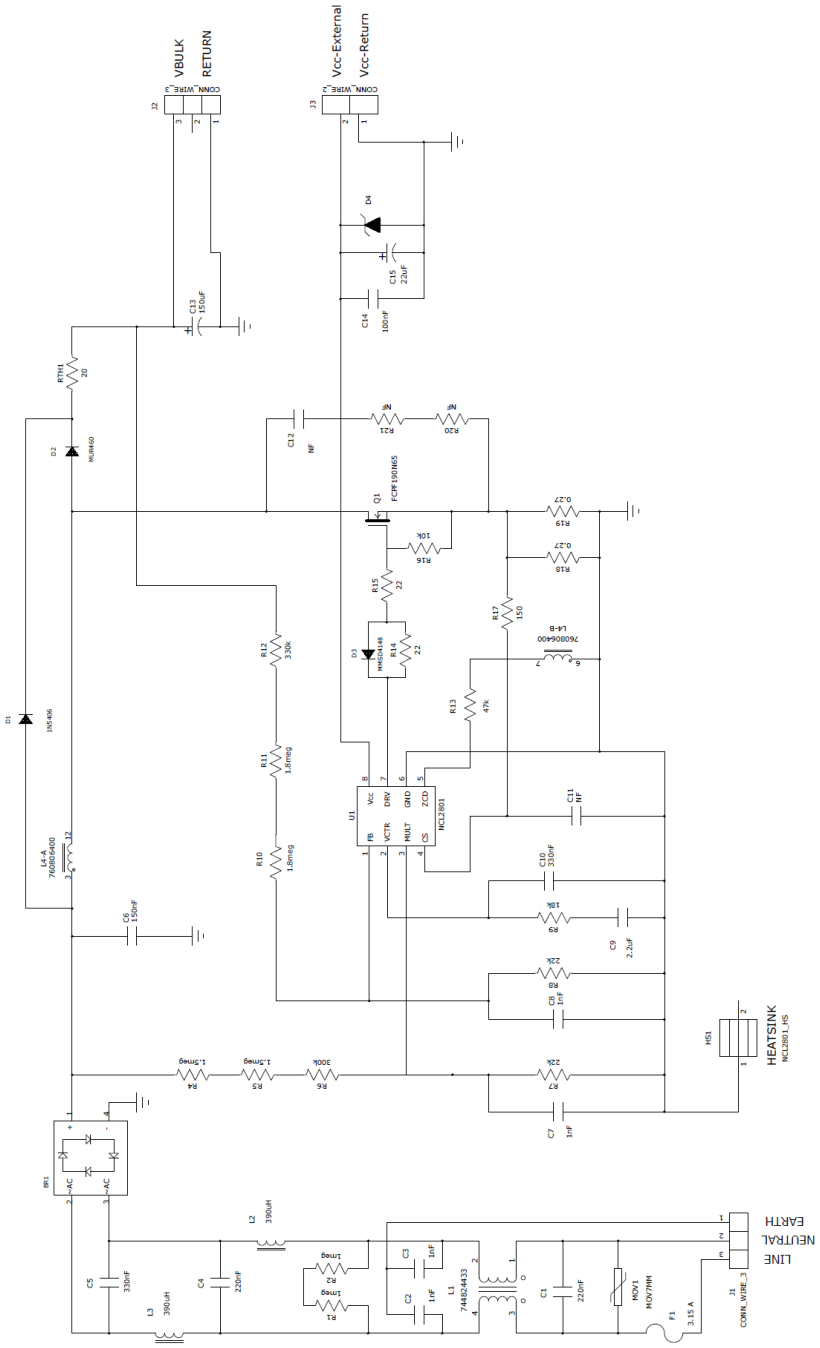


Figure 1. Schematic

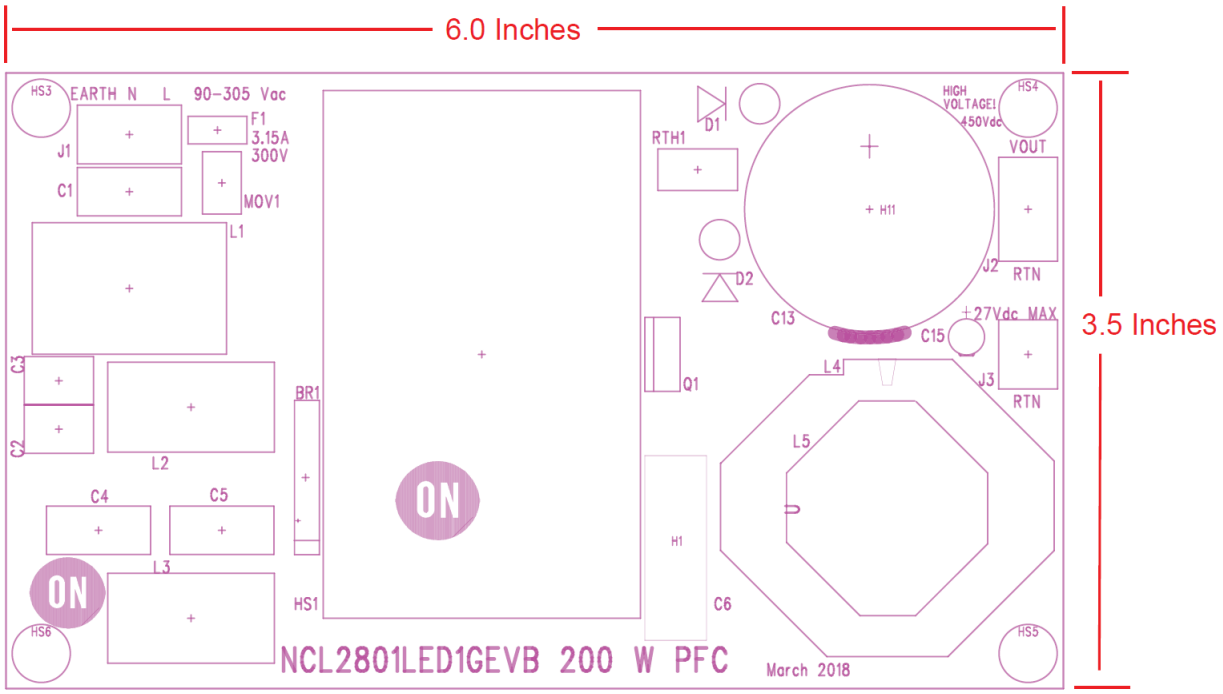


Figure 2. PCB Outline and Top Silkscreen

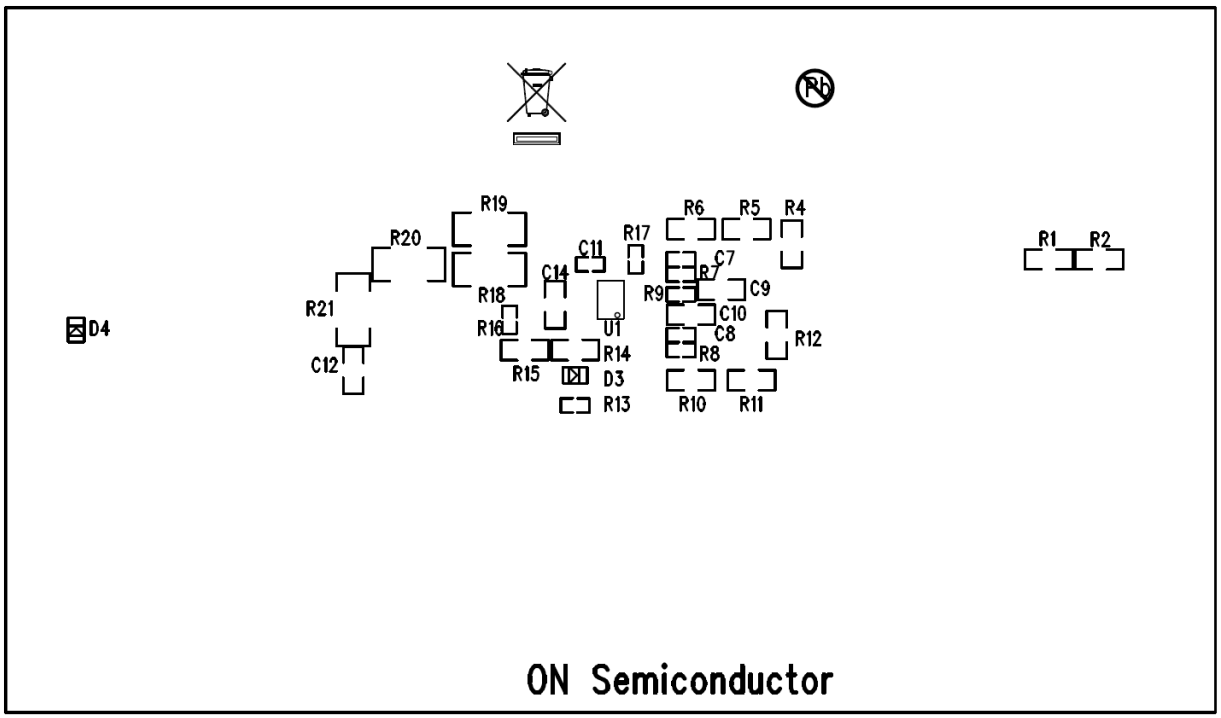


Figure 3. Bottom Silkscreen

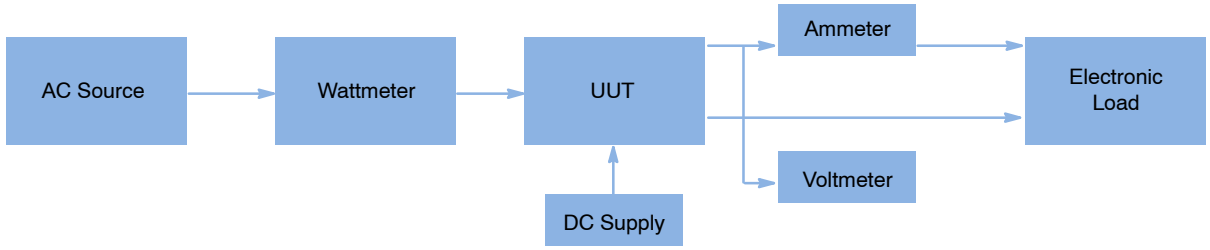
TEST PROCEDURE

Required Equipment

- AC Source – 90 to 277 V ac 50/60 Hz, Minimum 250 W capability
- AC Wattmeter – 250 W Minimum, THDi measurement capability
- DC Voltmeter – 500 V dc Minimum, 0.1% accuracy
- DC Ammeter – 1 A dc Minimum, 0.1% accuracy
- Adjustable DC lab supply, 13 V dc, 100 mA minimum
- Electronic Load, 500 V dc, 250 W MinimumTest Connections

Test Connections

1. Connect AC power to the input of the wattmeter. Connect output of wattmeter to input connector J1 of UUT. Connect J1 Earth to ground for safety.
2. Connect UUT output connector J2 'Vout' to DC ammeter. Connect other lead of DC ammeter to "+" of electronic load. Connect UUT output connector J2 'RTN' to "−" of electronic load.
3. Connect DC voltmeter to UUT output connector J2 'Vout' and 'RTN'.
4. Connect UUT bias connector J3 '+27Vdc Max' to "+" lead of DC lab supply. Connect UUT bias connector J3 'RTN' to "−" lead of DC lab supply.



NOTE: Unless otherwise specified, all voltage measurements are taken at the terminals of the UUT.

Figure 4. Test Setup

No Load Test

1. Apply 13 V dc to Vcc connector J3
2. Set electronic load to zero amps
3. Apply 230 V ac to input connector J1.
   Caution: Do not touch the UUT once it is energized. Hazardous voltages are present.
4. Verify Output Voltage is 436.5 to 463.5 V dc
5. Set input voltage on J1 to zero volts, Set Vcc on J3 to zero volts

Load Test

1. Set electronic load to 0.443 Amps (full load)
2. Apply 90 V ac to input connector J1.
   Caution: Do not touch the UUT once it is energized. Hazardous voltages are present.
3. Apply 13 V dc to Vcc connector J3
4. Verify performance per table below. (THDi is input current distortion)
5. Apply 277 V ac to input connector J1. Verify performance per table below.

Input Voltage	Input Power	THDi	Output Voltage	Output Current
90	< 229 W	< 6%	436.5 to 463.5 V	0.435 to 0.450 A
277	< 217 W	< 5%	436.5 to 463.5 V	0.435 to 0.450 A

6. Set ac input voltage on connector J1 to zero.
7. Set bias power on Vcc connector J3 to zero.
8. **Ensure Vout < 30 V dc before handling UUT.**

Test Complete

TYPICAL TEST DATA

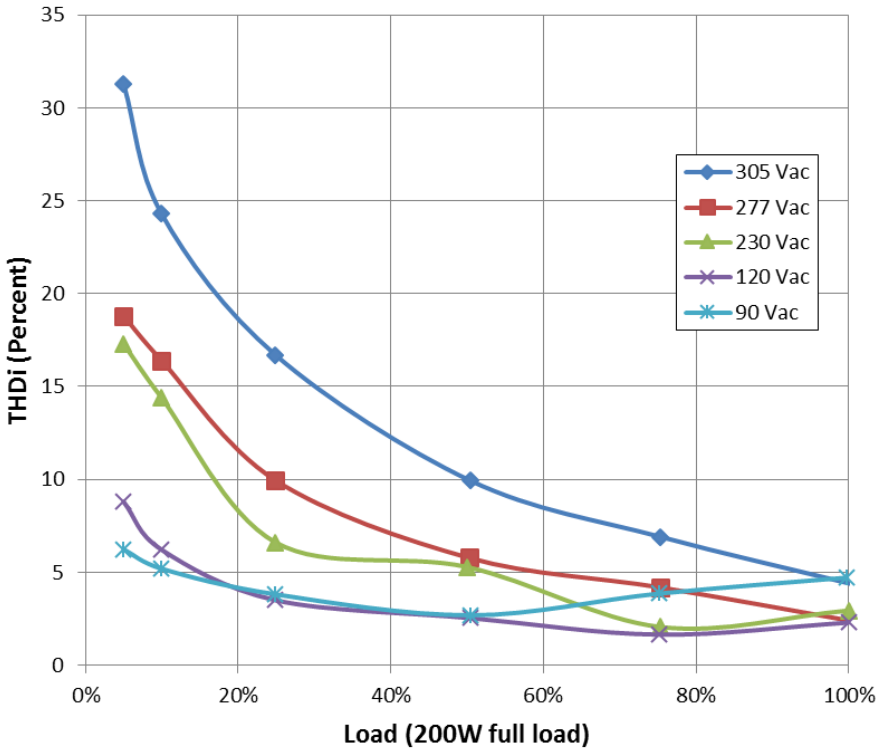


Figure 5. THDi Performance

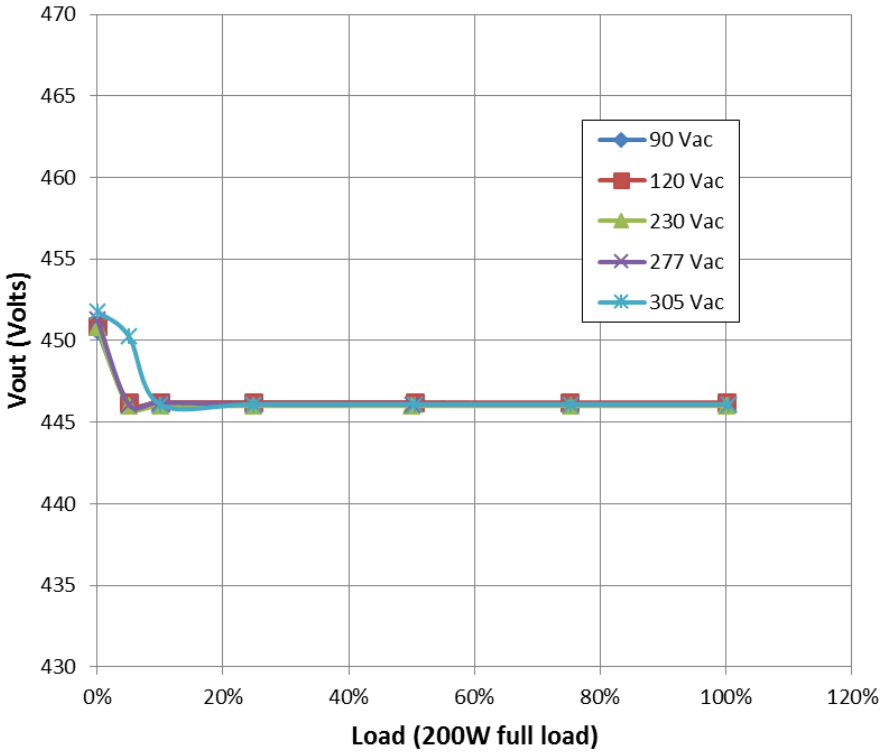


Figure 6. Line and Load Regulation Performance

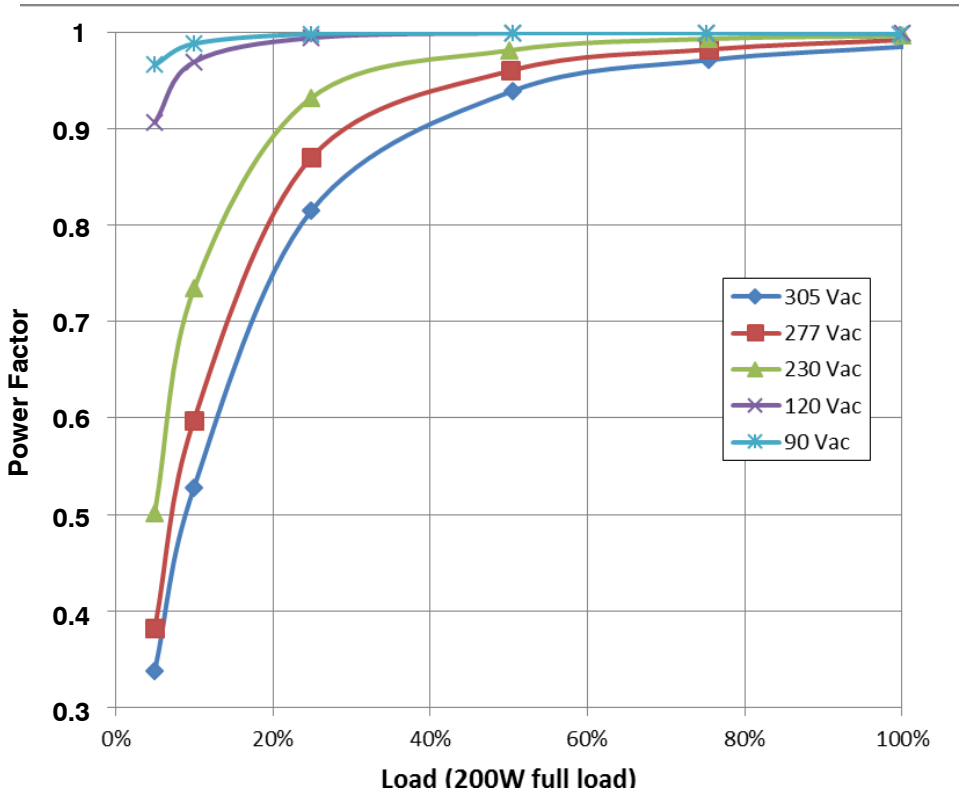


Figure 7. Power Factor Performance

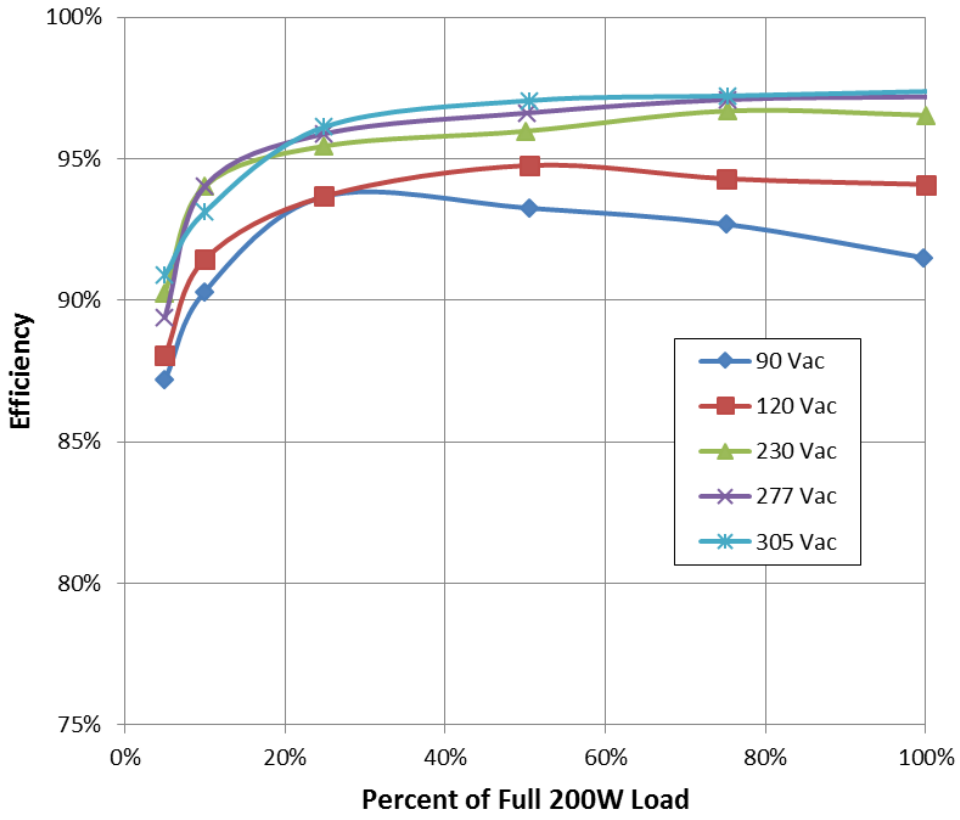


Figure 8. Efficiency

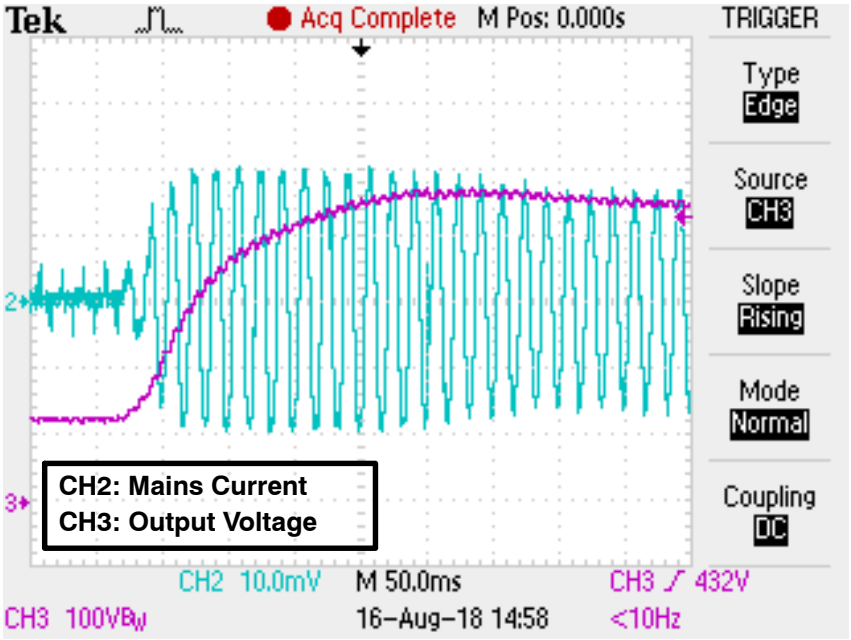


Figure 9. 90 V ac Full Load Startup

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